SGS-THOMSON MICROELECTRONICS

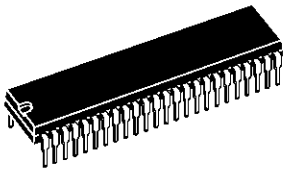
MK50H25

HIGH SPEED LINK LEVEL CONTROLLER

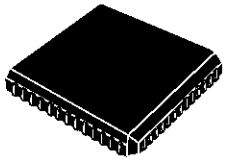
ADVANCE DATA

SECTION 1 - FEATURES

- System clock rate up to 33 MHz (MK50H25 - 33), 25 MHz (MK50H25 - 25), or 16 MHz (MK50H25 - 16).
- Data rate up to 20 Mbps continuous (MK50H25 - 33) or up to 51 Mbps bursted
- On chip DMA control with programmable burst length.
- DMA transfer rate of up to 13.3 Mbytes/sec using optional 5 SYSCLK DMA cycle (150 nS) at 33 MHz SYSCLK.
- Complete Level 2 implementation compatible with X.25 LAPB, ISDN LAPD, X.32, and X.75 Protocols.
  Handles all error recovery, sequencing, and S and U frame control.
- Pin-for-pin and architecturally compatible with MK5025 (X.25/LAPD), MK5027 (CCS#7) and MK5029(SDLC).
- Buffer Management includes:
  - Initialization Block
  - Separate Receive and Transmit Rings
  - Variable Descriptor Ring and Window Sizes.
- Separate 64-byte Transmit and Receive FIFO.
- Programmable Transmit FIFO hold-off watermark.
- Handles all HDLC frame formatting:
  - Zero bit insertion and deletion
  - FCS (CRC) generation and detection
  - Frame delimiting with flags
- Programmable Single or Extended Address and Control fields.
- Five programmable timer/counters: T1, T3, TP, N1, N2
- Programmable minimum frame spacing on transmission (number of flags between frames).
  - Programmable from 1 to 62 flags between frames
- Selectable FCS (CRC) of 16 or 32 bits, and passing of entire FCS to buffer.
- Testing Facilities:
  - Internal Loopback
  - Silent Loopback
  - Optional Internal Data Clock Generation
  - Self Test.
- Programmable for full or half duplex operation



DIP48



PLCC 52

- Programmable Watchdog Timers for RCLK and TCLK (to detect absence of data clocks)
- Option causing received data to effectively be odd-byte aligned, in addition to standard even-byte alignment.
- Available in 52 pin PLCC, 84 pin PLCC(for use with external ROM), or 48 pin DIP packages.

SECTION 2 - INTRODUCTION

The SGS - Thomson MK502H5 Link Level Controller is a VLSI semiconductor device which provides complete link level data communications control conforming to the 1984 and 1988 CCITT versions of X.25. The MK50H25 will perform frame formating including: frame delimiting with flags, transparency (so-called ”bit-stuffing”), error recovery by retransmission, sequence number control, S (supervisory) and U (unnumbered) frame control, plus FCS (CRC) generation and detection. The MK50H25 also supports X.75 and X.32 (with its XID frame support), as well as single channel ISDN LAPD (with its support of UI frames and extended addressing capabilities).

DESCRIPTION (Continued)

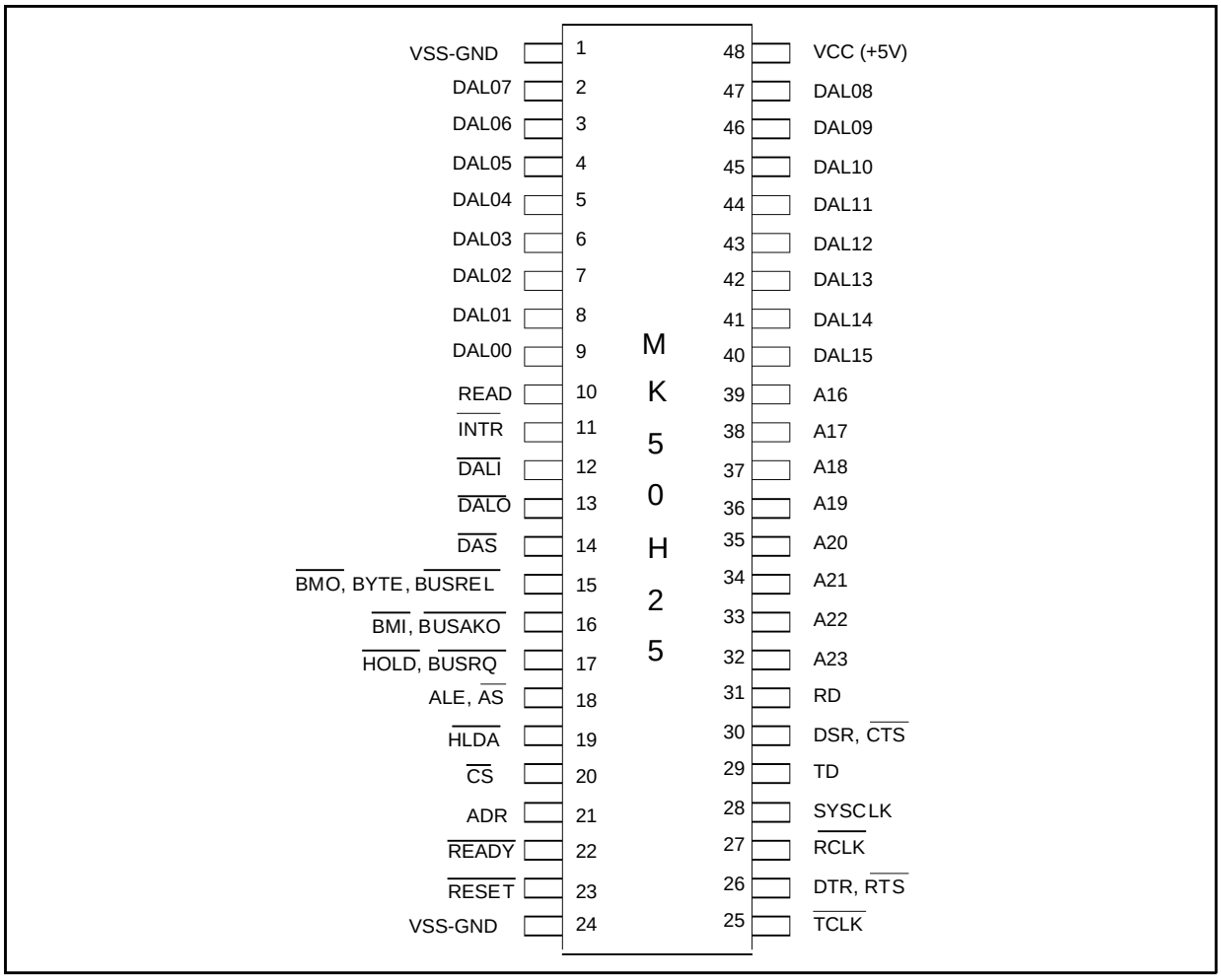
For added flexibility a transparent mode provides an HDLC transport mechanism without link layer support. This flexible transparent mode may be easily entered and exited without affecting the X.25 link status or the link state variables kept by the MK50H25. In this mode no protocol processing is done and it is up to the user to take care of the upper level software. Single or extended Address field filtering and Control field handling are optionally supported within the transparent mode.

One of the outstanding features of the MK50H25 is its buffer management which includes on-chip dual channel DMA. This feature allows users to receive and transmit multiple data frames at a time. (A conventional serial communications control chip plus a separate DMA chip would handle data for only a single block at a time.) The MK50H25 will move multiple blocks of receive and transmit data directly into and out of memory through the Host's bus. A possible system configuration for the MK50H25 is shown in figure 1.

The MK50H25 may be used with any of several popular 16 and 8 bit microprocessors, such as 68020, 68000, 6800, Z8000, Z80, 8086, 8088, 80186, 80286, 80386SX, etc.

The MK50H25 may be operated in either full or half duplex mode. In half duplex mode, the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins. All signal pins on the MK50H25 are TTL compatible. This has the advantage of making the MK50H25 independent of the physical interface. As shown in figure 1, line drivers and receivers are used for electrical connection to the physical layer.

DIP48 PIN CONNECTION (Top view)



PLCC52 PIN CONNECTION (Top view)

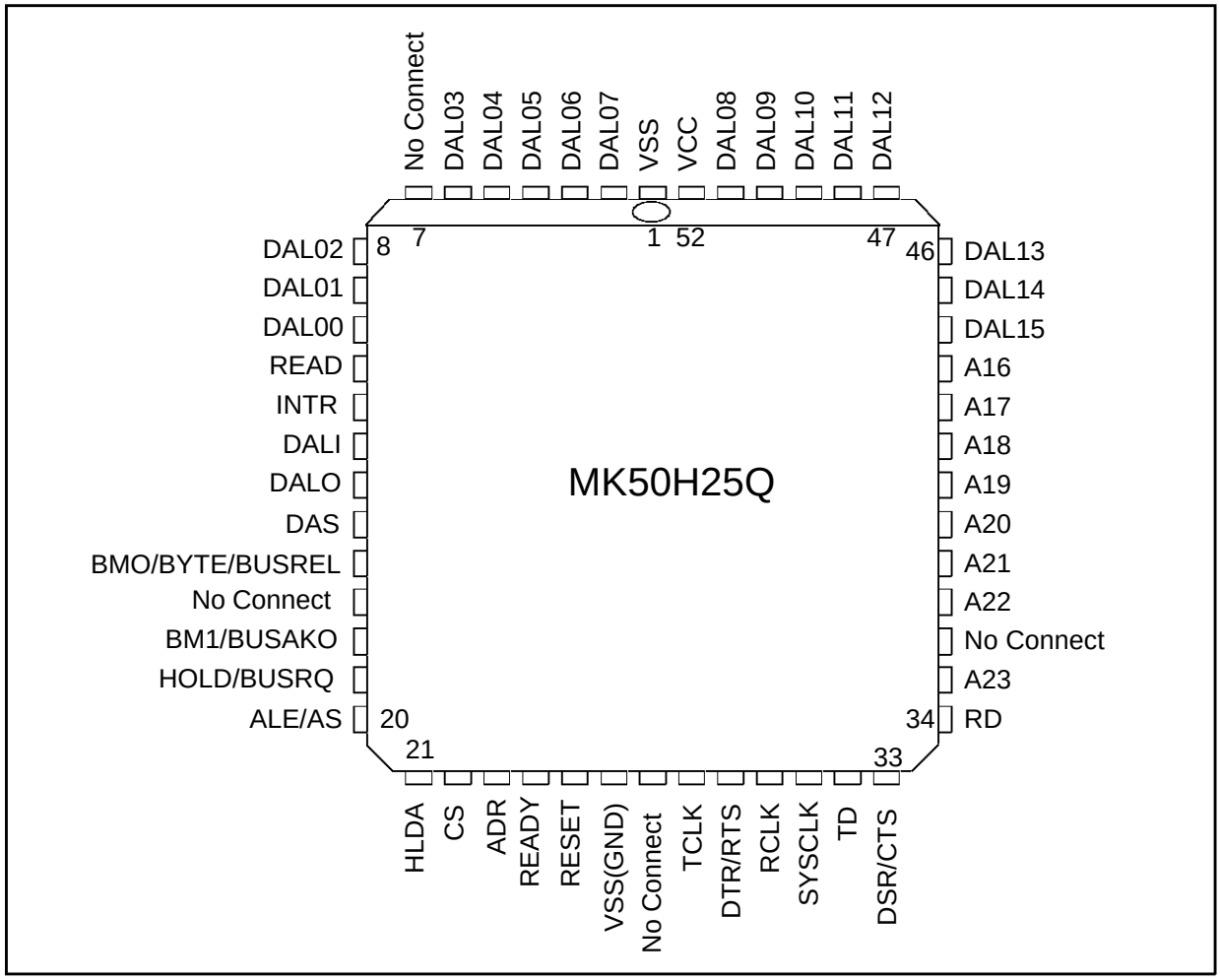


TAble 1: PIN DESCRIPTION

LEGEND:

I	Input only	O	Output only
IO	Input / Output	3S	3-State
OD	Open Drain (no internal pull-up)		

Note: Pin out for 52 pin PLCC is shown in brackets.

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
DAL<15:00>	2-9 40-47 [2-10 44-51]	IO/3S	The time multiplexed Data/Address bus. During the address portion of a memory transfer, DAL<15:00> contains the lower 16 bits of the memory address. During the data portion of a memory transfer, DAL<15:00> contains the read or write data, depending on the type of transfer.
READ	10 [11]	IO/3S	READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK50H25 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated at all other times. MK50H25 as a Bus Slave : READ = HIGH - Data is placed on the DAL lines by the chip. READ = LOW - Data is taken off the DAL lines by the chip. MK50H25 as a Bus Master : READ = HIGH - Data is taken off the DAL lines by the chip. READ = LOW - Data is placed on the DAL lines by the chip.
INTR	11 [12]	O/OD	INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set: MISS, MERR, RINT, TINT or PINT. INTERRUPT is enabled by CSR0<09>, INEA=1.
DALI	12 [13]	O/3S	DAL IN is an external bus transceiver control line. DALI is driven by the MK50H25 only while it is the BUS MASTER. DALI is asserted by the MK50H25 when it reads from the DAL lines during the data portion of a READ transfer. DALI is not asserted during a WRITE transfer.
DALO	13 [14]	O/3S	DAL OUT is an external bus transceiver control line. DALO is driven by the MK50H25 only while it is the BUS MASTER. DALO is asserted by the MK50H25 when it drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer.
DAS	14 [15]	IO/3S	DATA STROBE defines the data portion of a bus transaction. By definition, data is stable and valid at the low to high transition of DAS. This signal is driven by the MK50H25 while it is the BUS MASTER. During the BUS SLAVE operation, this pin is used as an input. At all other times the signal is tristated.
BMO BYTE BUSREL	15 [16]	IO/3S	I/O pins 15 and 16 are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 becomes input BUSREL and is used by the host to signal the MK50H25 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear then pin 15 is an output and behaves as described below for pin 16.
BM1 BUSAKO	16 [18]	O/3S	Pins 15 and 16 are programmable through bit 00 of CSR4 (BCON). If CSR4<00> BCON = 0, I/O PIN 15 = BMO (O/3S) I/O PIN 16 = BM1 (O/3S) BYTE MASK<1:0> Indicates the byte(s) on the DAL to be read or written during this bus transaction. MK50H25 drives these lines only as a Bus Master. MK50H25 ignores the BM lines when it is a Bus Slave. Byte selection is done as outlined in the following table. BM1 BM0 TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH UPPER BYTE (DAL<15:08>) HIGH LOW LOWER BYTE (DAL<07:00>) HIGH HIGH NONE

Table 1: PIN DESCRIPTION (continued)

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
			If CSR4<00> BCON = 1, I/O PIN 15 = BYTE (O/3S) I/O PIN 16 = BUSAKO(O) Byte selection is done using the BYTE line and DAL<00> latched during the address portion of the bus transaction. MK50H25 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table. BYTE DAL<00> TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH ILLEGAL CONDITION HIGH LOW LOWER BYTE HIGH HIGH UPPER BYTE BUSAKO is a bus request daisy chain output. If MK50H25 is not requesting the bus and it receives HLDA, BUSAKO will be driven low. If MK50H25 is requesting the bus when it receives HLDA, BUSAKO will remain high Note: All transfers are entire word unless the MK50H25 is configured for 8 bit operation.
HOLD BUSRQ	17 [19]	IO/OD	Pin 17 is configured through bit 0 of CSR4. If CSR4<00> BCON = 0, I/O PIN 17 = HOLD HOLD request is asserted by MK50H25 when it requires a DMA cycle, if HLDA is inactive, regardless of the previous state of the HOLD pin. HOLD is held low for the entire ensuing bus transaction. If CSR4<00> BCON = 1, I/O PIN 17 = BUSRQ BUSRQ is asserted by MK50H25 when it requires a DMA cycle if the prior state of the BUSRQ pin was high and HLDA is inactive. BUSRQ is held low for the entire ensuing bus transaction.
ALE AS	18 [20]	O/3S	The active level of ADDRESS STROBE is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by MK50H25 while it is the BUS MASTER. At all other times, the signal is tristated. If CSR4<01> ACON = 0, I/O PIN 18 = ALE ADDRESS LATCH ENABLE is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion. If CSR4<01> ACON = 1, I/O PIN 18 = AS As AS, the signal pulses low during the address portion of the bus transfer. The low to high transition of AS can be used by a slave device to strobe the address into a register. AS is effectively the inversion of ALE.
HLDA	19 [21]	I	HOLD ACKNOWLEDGE is the response to HOLD. When HLDA is low in response to MK50H25's assertion of HOLD, the MK50H25 is the Bus Master. HLDA should be deasserted ONLY after HOLD has been released by the MK50H25.
CS	20 [22]	I	CHIP SELECT indicates, when low, that the MK50H25 is the slave device for the data transfer. CS must be valid throughout the entire transaction.
ADR	21 [23]	I	ADDRESS selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when CS is low. ADR PORT LOW REGISTER DATA PORT HIGH REGISTER ADDRESS PORT
READY	22 [24]	IO/OD	When the MK50H25 is a Bus Master, READY is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle.

Table 1: PIN DESCRIPTION (continued)

SIGNAL NAME	PIN(S)	TYPE	DESCRIPTION
			As a Bus Slave, the MK50H25 asserts READY when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during a WRITE cycle. READY is a response to DAS and it will be released after DAS or CS is negated.
RESET	23 [25]	I	RESET is the Bus signal that will cause MK50H25 to cease operation, clear its internal logic and enter an idle state with the Power Off bit of CSR0 set.
TCLK	25 [28]	I	TRANSMIT CLOCK. A 1x clock input for transmitter timing. TD changes on the falling edge of TCLK. The frequency of TCLK may not be greater than the frequency of SYSCL
DTR RTS	26 [29]	IO	DATA TERMINAL READY, REQUEST TO SEND. Modem control pin. Pin 26 is configurable through CSR5. This pin can be programmed to behave as output RTS or as programmable IO pin DTR. If configured as RTS, the MK50H25 will assert this pin if it has data to send and throughout the transmission of a signal unit.
RCLK	27 [30]	I	RECEIVE CLOCK. A 1x clock input for receiver timing. RD is sampled on the rising edge of RCLK. The frequency of RCLK may not be greater than the frequency of SYSCLK.
SYSCLK	28 [31]	I	SYSTEM CLOCK. System clock used for internal timing of the MK50H25. SYSCLK should be a square wave, of frequency up to 33 MHz.
TD	29 [32]	O	TRANSMIT DATA. Transmit serial data output.
DSR CTS	30 [33]	IO	DATA SET READY, CLEAR TO SEND. Modem Control Pin. Pin 30 is configurable through CSR5. This pin can be programmed to behave as input CTS or as programmable IO pin DSR. If configured as CTS, the MK50H25 will transmit all ones while CTS is high.
RD	31 [34]	I	RECEIVE DATA. Received serial data input.
A<23:16>	32-39 [37-43]	o/3s	Address bits <23:16> used in conjunction with DAL<15:00> to produce a 24 bit address. MK50H25 drives these lines only as a Bus Master. A23-A20 may be driven continuously as described in the CSR4<7> BAE bit.
VSS-GND	1,24 [1,26]		Ground Pins
VCC	48 [52]		Power Supply Pin +5.0 VDC ± 5%

SECTION 3
OPERATIONAL DESCRIPTION

The SGS-Thomson MK50H25 Multi-Logical Link Communications Controller device is a VLSI product intended for high performance data communication applications requiring X.25 link level control. The MK50H25 will perform all frame formatting, such as: frame delimiting with flags, FCS (CRC) generation and detection, and zero bit insertion and deletion for transparency. The MK50H25 also handles all supervisory (S) and unnumbered (U) frames (see Tables A & B). The MK50H25 also includes a buffer management mechanism that allows the user to transmit and/or receive multiple frames for each active channel or DLCI. Contained in the buffer management is an on-chip dual channel DMA: one channel for receive and one channel for transmit.

The MK50H25 can be used with any popular 16 or 8 bit microprocessor. A possible system configuration for the MK50H25 is shown in Figure 1. This document assumes that the processor has a byte addressable memory organization.

The MK50H25 will move multiple blocks of receive and transmit data directly in and out of memory through the Host's bus.

The MK50H25 may be operated in full or half duplex mode. In half duplex mode the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins.

All signal pins on the MK50H25 are TTL compatible. This has the advantage of making the MK50H25 independent of the physical interface. As shown in Fig. 1, line drivers and receivers are used for electrical connection to the physical layer.

Figure 1: Possible System Configuration for thr MK50H25

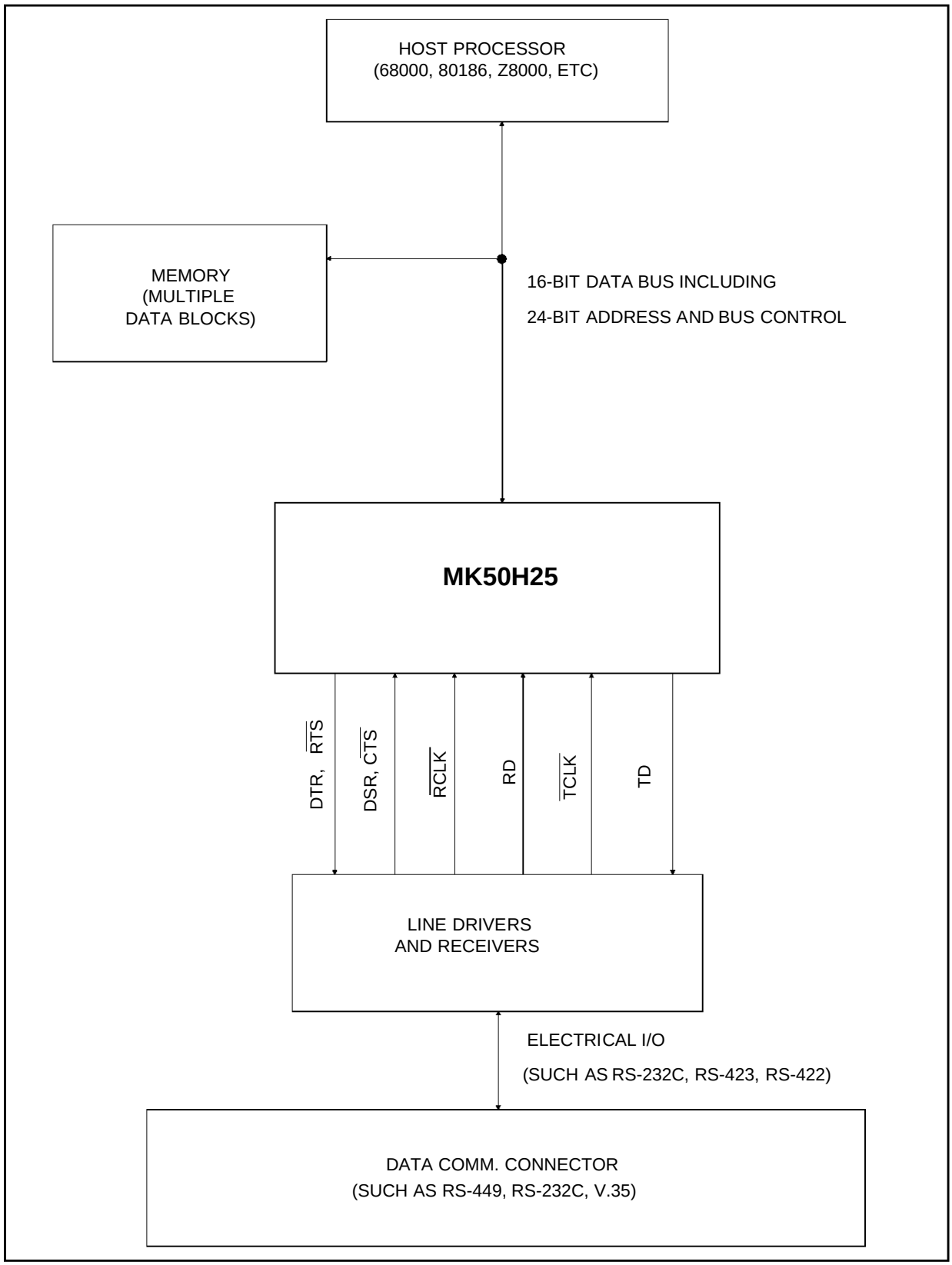
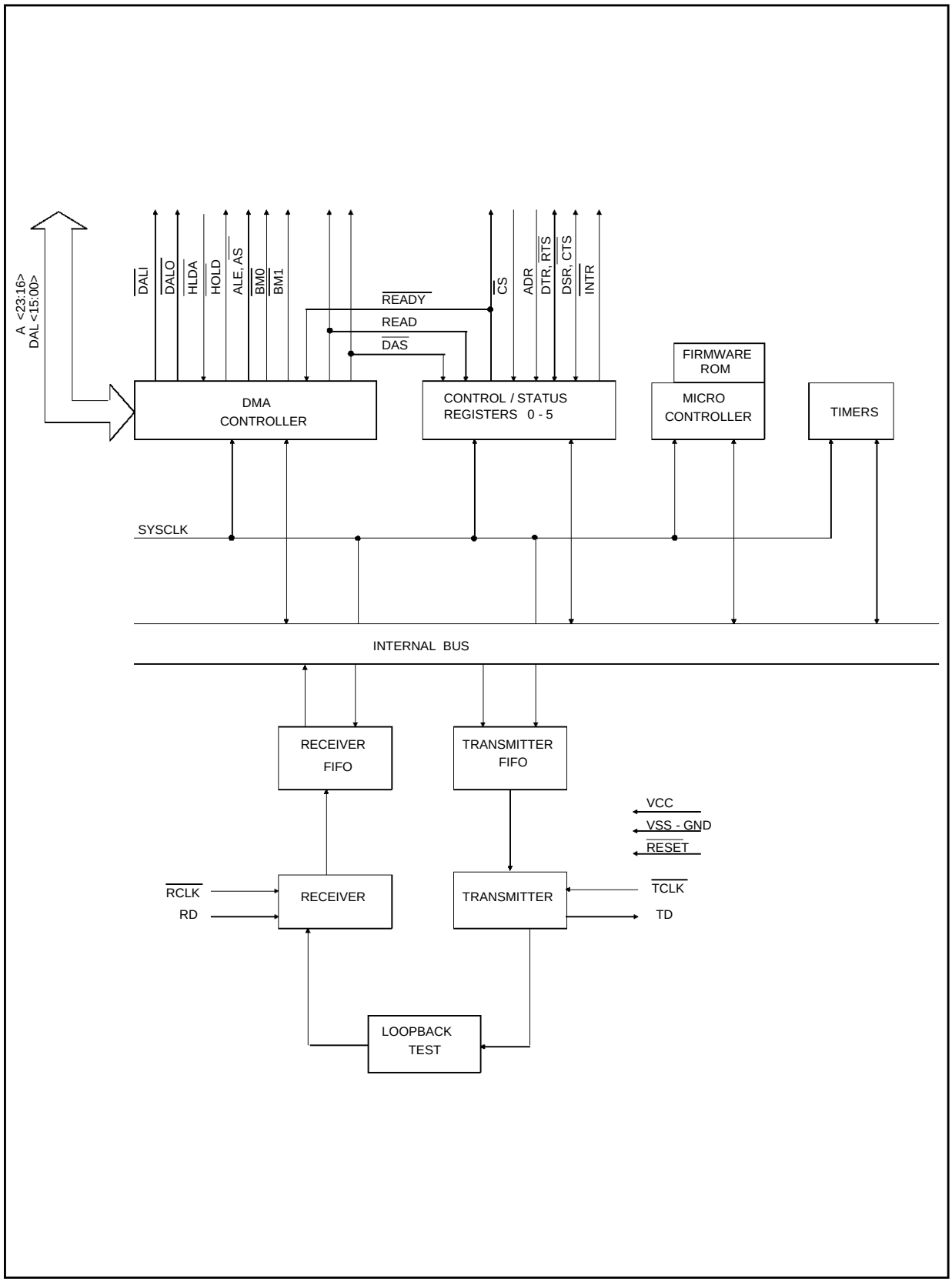


Figure 2: MK50H25 Simplified Block Diagram



3.1 Functional Blocks

Refer to the block diagram in Figure 2.

The MK50H25 is primarily initialized and controlled through six 16-bit Control and Status Registers (CSR0 thru CSR5). The CSR's are accessed through two bus addressable ports, the Register Address Port (RAP), and the Register Data Port (RDP). The MK50H25 may also generate an interrupt(s) to the Host. These interrupts are enabled and disabled through CSR0.

The on-chip microcontroller is used to control the movement of parallel receive and transmit data, and to handle the Address field filtering.

3.1.1 Microcontroller

The microcontroller controls all of the other blocks of the MK50H25. The microcontroller performs frame processing and protocol processing. All primitive processing and generation is also done here. The microcode ROM contains the control program of the microcontroller.

3.1.2 Receiver

Serial receive data comes into the Receiver (Figure 2). The Receiver is responsible for:

1. Leading and trailing flag detection.
2. Deletion of zeroes inserted for transparency.
3. Detection of idle and abort sequences.
4. Detection of good and bad FCS (CRC).
5. Monitoring Receiver FIFO status.
6. Detection of Receiver Over-Run.
7. Odd byte detection.

   NOTE: If frames are received that have an odd number of bytes then the last byte of the frame is said to be an odd byte.

8. Detection of non-octet aligned frames. Such frames are treated as invalid (CCITT X.25 sec 2.3.5.3)

3.1.3 Transmitter

The Transmitter is responsible for:

1. Serialization of outgoing data.
2. Generating and appending the FCS (CRC).
3. Framing outgoing frame with flags.
4. Zero bit insertion for transparency.
5. Transmitter Under-Run detection.
6. Transmission of odd byte.
7. RTS/CTS control.

3.1.4 Frame Check Sequence or Cyclic Redundancy Check

The FCS (CRC) on the transmitter or receiver may be either 16 bit or 32 bit, and is user selectable. For full duplex operation, both the receiver and transmitter have individual FCS computation circuits. The characteristics of the FCS are:

Transmitted Polarity: Inverted

Transmitted Order: High Order Bit First

Pre-set Value: All 1's

Polynomial 16 bit:
$X^{16} + X^{12} + X^5 + 1$

Remainder 16 bit (if received correctly):
High order bit-->0001 1101 0000 1111

Polynomial 32 bit:
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

Remainder 32 bit (if received correctly):
high order bit-->1100 0111 0000 0100
1101 1101 0111 1011

3.1.5 Receive FIFO

The Receive FIFO buffers the data received by the receiver. This performs two major functions. First, it resynchronizes the data from the receive clock to the system clock. Second, it allows the microcontroller time to finish whatever it may be doing before it has to process the received data.

The receive FIFO holds the data from the receiver without interrupting the microcontroller for service until it contains enough data to reach the watermark level, or an end of frame is received. This watermark level can be programmed in CSR4 (FWM) to occur when the FIFO contains at least 18 or more bytes; 34 or more bytes; or 50 or more bytes. This programmability , along with the programmable burst length of the DMA controller, enables the user to define how often and for how long the MK50H25 must use the host bus. For more information, see CSR4.

For example, if the watermark level is set at 34 bytes and the burst length is limited to 8 word transfers at a time, the MK50H25 will request control of the host bus as soon as 34 bytes are received and again after every 16 subsequent bytes.

3.1.6 Transmit FIFO

The Transmit FIFO buffers the data to be transmitted by the MK50H25. This also performs two major functions. First, it resynchronizes the data from the system clock to the transmit clock. Second, it allows the microcontroller and DMA controller to burst read data from the host's memory buffers; making both the MK50H25 and the host bus more efficient.

The transmit FIFO has a watermark scheme similar to the one described for the receive FIFO above, and uses the same FWM value selections in CSR4 for the watermark. Once filled to within

FWM of being full (by DMA from TX buffer in shared memory), the transmit FIFO will not interrupt the microcontroller until it empties enough to fall below the watermark level.

The transmit FIFO also has a selectable Transmit Hold-Off watermark mechanism to determine when data transmission will begin once data has been put in the transmit FIFO. The Transmit Hold-Off watermark is enabled by setting bit 10 (XHOLD) in CSR4. The selection of FWM (FIFO WaterMark) also in CSR4 determines corresponding appropriate values of Transmit Hold-Off so that the device cannot be inadvertently programmed to have conflicting watermarks. For FWM settings of 9, 17, and 25 words, the Transmit Hold-Off watermarks are 19, 11, and 3 words respectively.

For example, if FWM is set at 9 words and the Transmit Hold-Off watermark is enabled, the MK50H25 will not begin transmitting until more than 19 words have been placed in the Transmit FIFO or an end-of-frame has been transmitted. This greatly reduces the chances of Transmitter Underrun that could be possible at high data rates (ie: TCLK > 0.15 x SYSCLK) if Transmit Hold-Off is not selected (causing transmission to begin as soon as 1 byte is transferred to the TX FIFO).

3.1.7 DMA Controller

The MK50H25 has an on-chip DMA Controller circuit. This allows it to access memory without requiring host software intervention. Whenever the MK50H25 requires access to the host memory it will negotiate for mastership of the bus. Upon gaining control of the bus the MK50H25 will begin transferring data to or from memory. The MK50H25 will perform memory transfers until either it has nothing more to transfer, it has reached its DMA burst limit (user programmable), or the BUSREL pin is driven low. In any case, it will complete all bus transfers before releasing bus mastership back to the host. If during a memory transfer, the memory does not respond within 256 SCLK cycles, the MK50H25 will release ownership of the bus immediately and the MERR bit will be set in CSR0. The DMA burst limit can be programmed by the user through CSR4. In 16 bit mode the limit can be set to 1 word, 8 words, or unlimited word transfers. In 8 bit mode,it can be set to 2 bytes, 16 bytes, or unlimited byte transfers. For high speed data lines (i.e. > 1 Mbps) a burst limit of 8 words or 16 bytes is suggested to allow maximum throughput.

The byte ordering of the DMA transfers can be programmed to account for differences in processor architectures or host programming languages. Byte ordering can be programmed separately for data and control information. Data information is defined as all contents of data buffers; control information is defined as anything else in the shared memory space (i.e. initialization block, descriptors, etc). For more information see section 4.1.2.5 on control status register 4.

3.1.8 Bus Slave Circuitry

The MK50H25 contains a bank of internal control/status registers (CSR0-5) which can be accessed by the host as a peripheral. The host can read or write to these registers like any other bus slave. The contents of these registers are listed in Section 4 and bus signal timing is described in Figures 9 and 10.

3.2 Buffer Management Overview

Refer to Fig. 3.

3.2.1 Initalization Block

Chip initialization information is located in a block of memory called the Initialization Block. The Initialization Block consists of 25 contiguous words of memory starting on a word boundary. This memory is assembled by the HOST, and is accessed by the MK50H25 during initialization. The Initialization Block is comprised of:

A. Mode of Operation.

B. Frame Address Values.

C. N1 Counter (Max Frame Length) Value.

D. Timer Preset Values

E. Location and size of Receive and Transmit Descriptor Rings.

F. Location and size of XID/TEST Buffers.

G. Location of Status Buffer.

H. Error Counters.

3.2.2 The Circular Queue

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK50H25. The descriptor ring has a descriptor assigned to each buffer. Each descriptor holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in bytes.

Each descriptor also contains two control bits called OWNA and OWNB, which denote whether the MK50H25, the HOST, or the I/O ACCELERATION PROCESSOR (if present) "owns" the buffer. For transmit, when the MK50H25 owns the buffer, the MK50H25 is allowed and commanded to transmit the buffer. When the MK50H25 does not own the buffer, it will not transmit that buffer. For receive, when the MK50H25 owns a buffer, it may place received data into that buffer. Conversely, when the MK50H25 does not own a receive buffer, it will not place received data into that buffer.

The MK50H25 buffer management mechanism will handle frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK50H25 tests the next descriptor in the de-

scriptor ring in a "look ahead" manner. If the frame is too long for one buffer, the next buffer will be used after filling the first buffer; that is, "chained". The MK50H25 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on.The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, frame Address field, etc. The starting address for the Initialization block, IADR, is defined in the CSR2 and CSR3 registers inside the MK50H25.

3.2.3 Frame Format

The frame format supported by the MK50H25 is shown below. Each frame may consist of a programmable number of leading flag patterns (01111110), an address field, a control field, an information field, an FCS (CRC) of either 16 or 32 bits, and a trailing flag pattern. The number of leading flags transmitted is programmable through the Mode Register in the Initialization Block. Received frames may have as few as one flag between adjacent frames

TRANSMITTED FIRST

F	A	C	INFO	FCS	F
8	8/16	8/16	8*n	16/32	8

3.2.4 The Command/Response Repertoire

The command/response repertoire of the MK50H25 is shown in Tables A and B. This set conforms to the 1984 & 1988 CCITT X.25, plus support of XID, Test, and UI frames conforming to ISDN LAPD. The MK50H25 will process the Information, Supervisory, and Unnumbered frames shown in Tables A and B, and will handle the A and C fields for all I and UI frames.

The symbols and definitions for the frame types are:

Name	Definition
I	Information frame
UI	Unnumbered Information frame
RR	Receiver Ready
RNR	Receiver Not Ready
REJ	Reject
FRMR	Frame Reject
UA	Unnumbered Acknowledge
SABM	Set Asynchronous Balance Mode
DISC	Disconnect
DM	Disconnect Mode
TEST	Link Test Frame
XID	Exchange Identification

Table A - MK50H25 Command/Response Repertoire
Modulo 8 Operation

FORMAT	COMMAND	RESPONSE	ENCODING LSB 1	2	3	4	5	6	7	MSB 8
Information Transfer	I	I	0	←	N(S)	→	P	←	N(R)	→
Supervisory	RR	RR	1	0	0	0	P/F	←	N(R)	→
	RNR	RNR	1	0	1	0	P/F	←	N(R)	→
	REJ	REJ	1	0	0	1	P/F	←	N(R)	→
Unnumbered	*UI	*UI	1	1	0	0	P/F	0	0	0
	SABM		1	1	1	1	P	1	0	0
		DM	1	1	1	1	F	0	0	0
	DISC		1	1	0	0	P	0	1	0
		UA	1	1	0	0	F	1	1	0
		FRMR	1	1	1	0	F	0	0	1
	*XID	*XID	1	1	1	1	P/F	1	0	1
	TEST	TEST	1	1	0	0	P/F	1	1	1

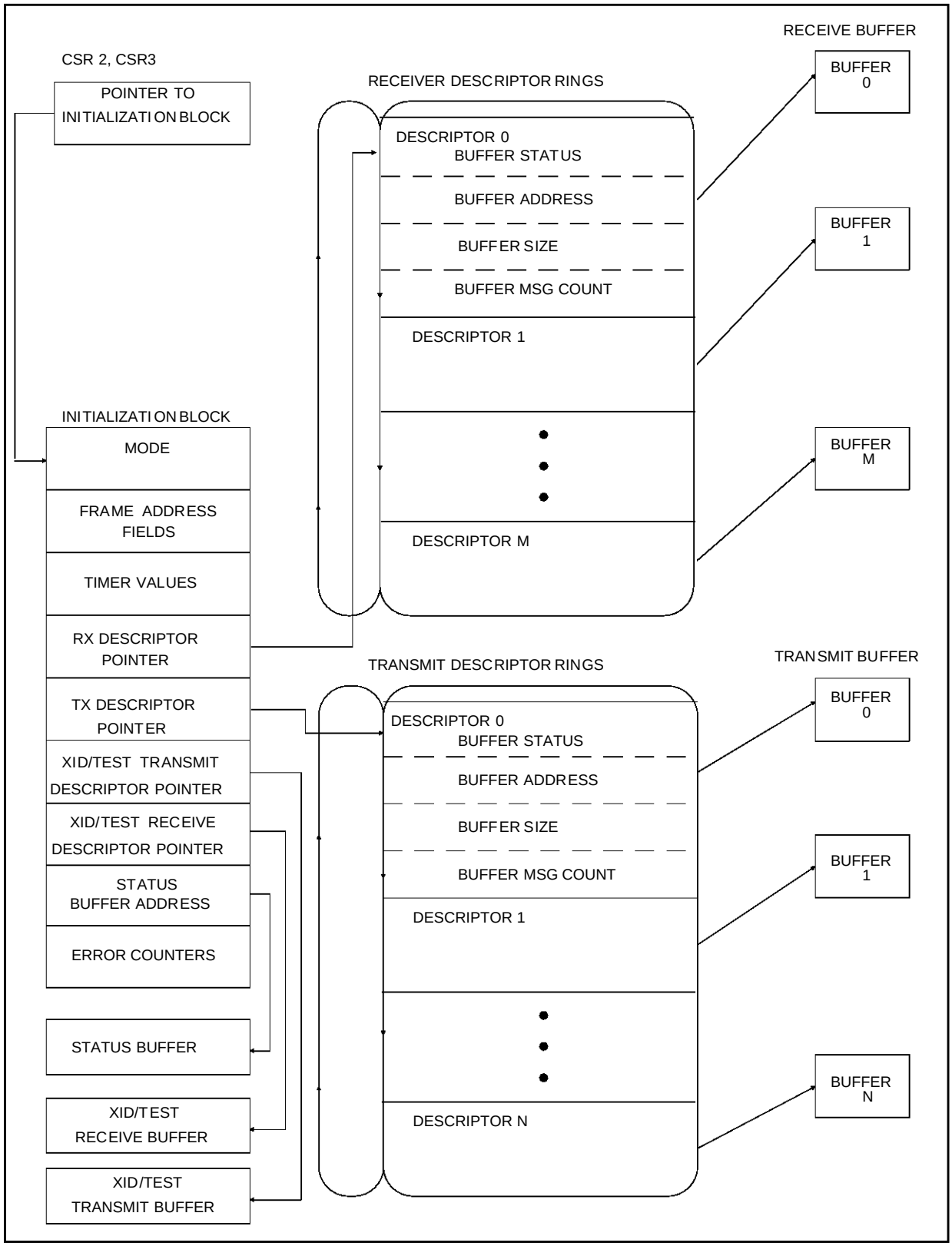
Table B - MK50H25 Command/Response Repertoire
Modulo 128 Operation

FORMAT	COMMAND	RESPONSE	ENCODING LSB 1	2	3	4	5	6	7	8	9	MSB 10-16
Information Transfer	I	I	0	←			N(S)			→	P	N(R)
Supervisory	RR	RR	1	0	0	0	0	0	0	0	P/F	N(R)
	RNR	RNR	1	0	1	0	0	0	0	0	P/F	N(R)
	REJ	REJ	1	0	0	1	0	0	0	0	P/F	N(R)
Unnumbered	SABME		1	1	1	1	P	1	1	0	N/A	
	All Others	All Others	Same Repertoire and Encoding as for Modulo 8									

Notes:
1. N(S) = Transmitter Send Sequence Number
2. N(R) = Transmitter Receive Sequence Number
3. P/F = Poll bit when issued as a command. Final bit when issued as a response.
4. N/A = Not Applicable. All Unnumbered frames have only an 8 bit Control Field for Modulo 128 or Modulo 8 operation.

*XID and UI frames can be enabled individually by setting the appropriate bits in CSR2.

Figure 3: MK50H25 Memory Management Structure



SECTION 4

PROGRAMMING SPECIFICATION

This section defines the Control and Status Registers and the memory data structures required to program the MK50H25.

4.1 Control and Status Registers

There are six Control and Status Registers (CSR's) resident within the MK50H25. The CSR's are accessed through two bus addressable ports, an address port (RAP), and a data port (RDP), thus requiring only two locations in the system memory or I/O map.

4.1.1 Accessing the Control & Status Registers

The CSR's are read (or written) in a two step operation. The address of the CSR is written into the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten or upon a bus reset. A control I/O pin (ADR) is provided to distinguish the address port from the data port.

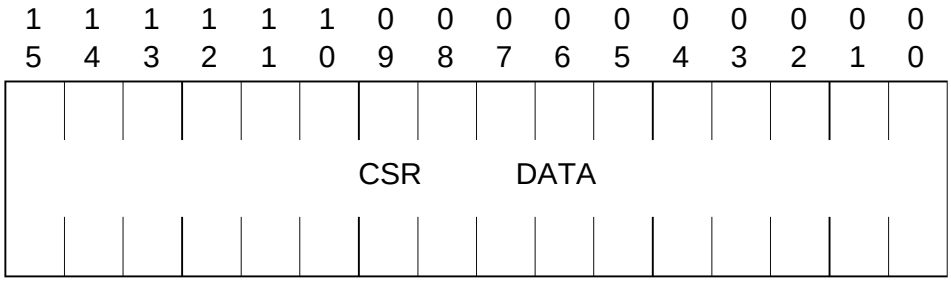
ADR	Port
L	Register Data Port (RDP)
H	Register Address Port (RAP)

4.1.1.1 Register Address Port (RAP)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	BM8	0	0	0	CSR <2:0>			HBYTE

BIT	NAME	DESCRIPTION
15:08	RESERVED	Must be written as zeroes
07	BM8	When set, places chip into 8 bit mode. CSR's, Init Block, and data transfers are all 8 bit transfers; this provides compatibility with 8 bitmicroprocessors. When clear, all transfers are 16 bit transfers. This bit must be set to the same value each time it is written, changing this bit during normal operation will achieve unexpected results. BM8 is READ/WRITE and cleared on Bus RESET.
06:04	RESERVED	Must be written as zeroes
03:01	CS3<2:0>	CSR address select bits. READ/WRITE. Selects the CSR to be accessed through the RDP. RAP is cleared by Bus RESET. CSR<2:0> CSR 0 CSR0 1 CSR1 2 CSR2 3 CSR3 4 CSR4 5 CSR5
00	HBYTE	Determines which byte is addressed for 8 bit mode. If set, the high byte of the register referred to by CSR<2:0> is addressed, otherwise the low byte is addressed. This bit is only meaningful in 8 bit mode and must be written as zero if BM8=0. HBYTE is READ/WRITE and cleared on bus reset.

4.1.1.2 Register Data Port (RDP)



BIT	NAME	DESCRIPTION
15:00	CSR DATA	Writing data to the RDP loads data into the CSR selected by RAP. Reading the data from RDP reads the data from the CSR selected in RAP.

4.1.2 Control and Status Register Definition

4.1.2.1 Control and Status Register 0 (CSR0)

RAP<3:1> = 0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PTDMD	STOP	DTX	DRX	TXON	RXON	INEA	INTR	MERR	MISS	ROR	TUR	PINT	TINT	RINT	0

BIT	NAME	DESCRIPTION
15	TDMD	TRANSMIT DEMAND, when set, causes the MK50H25 access the Transmit Descriptor Ring without waiting for the Transmit poll time interval to lapse. TDMD need not be set to transmit a frame, it merely hastens the MK50H25's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is written with ONE ONLY and cleared by the MK50H25 microcode after it is used. It may read as a "1" for a short time after it is written because the microcode may have been busy when TDMD was set. It is also cleared by Bus RESET. Writing a "0" in this bit has no effect.
14	STOP	STOP, when set, indicates that MK50H25 is operating in the Stopped phase of operation. All external activity is disabled and internal logic is reset. MK50H25 remains inactive except for primitive processing until a START primitive is issued. STOP IS READ ONLY and set by Bus RESET or a STOP primitive. Writing to this bit has no effect.
13	DTX	Disable Transmitter ring prevents the MK50H25 from further access to the Transmitter Descriptor Ring. No transmissions are attempted after finishing transmission of any frame in transmission at the time of DTX being set. TXON acknowledges changes to DTX, see below. DTX is READ/WRITE.
12	DRX	Disable the Receiver prevents the MK50H25 from further access to the Receiver Descriptor Ring. No received frames are accepted after finishing reception of any frame in reception at the time of DRX being set. If DRX is set while a data link is established, the MK50H25 will go into the Local Busy state and will send an RNR response frame to the remote station. Upon clearing DRX the MK50H25 will send a RR response frame. RXON acknowledges changes to DRX, see description of RXON. DRX is READ/WRITE.
11	TXON	TRANSMITTER ON indicates that the transmit ring access is enabled. TXON is set as the Start primitive is issued if the DTX bit is "0" or afterward as DTX is cleared. TXON is cleared upon recognition of DTX being set, by sending a Stop primitive in CSR1, or by a Bus RESET. If TXON is clear, the host may modify the Transmit Descriptor Ring entries regardless of the state of the OWNA bits. TXON is READ ONLY; writing to this bit has no effect.
10	RXON	RECEIVER ON indicates that the receive ring access is enabled. RXON is set as the Start primitive is issued if the DRX bit is "0" or afterward as DRX is cleared. RXON is cleared upon recognition of DRX being set, by sending a Stop primitive in CSR1, or by a Bus RESET. If RXON is clear, the host may modify the Receive Descriptor Ring entries regardless of the state of the OWNA bits. RXON is READ ONLY; writing to this bit has no effect.

09	INEA	INTERRUPT ENABLE allows the $\overline{\text{INTR}}$ I/O pin to be driven low when the Interrupt Flag is set. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ I/O pin will be low. If INEA = 0 the INTR I/O pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE set by writing a "1" into this bit and is cleared by writing a "0" into this bit, by Bus RESET, or by issuing a Stop primitive. INEA may not be set while in the Stopped phase.
08	INTR	INTERRUPT FLAG indicates that one or more of the following interrupt causing conditions has occurred: MISS, MERR, RINT, TINT, PINT, TUR or ROR. If INEA = 1 and INTR = 1 the INTR I/O pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared as the specific interrupting condition bits are cleared. INTR is also cleared by Bus RESET or by issuing a Stop primitive.
07	MERR	MEMORY ERROR is set when the MK50H25 is the Bus Master and READY has not been asserted within 256 SYSCLKs (25.6 usec @ 10MHz) after asserting the address on the DAL lines. When a Memory Error is detected, the MK50H25 releases the bus, the receiver and transmitter are turned off, and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a Stop primitive.
06	MISS	MISSED frame is set when the receiver loses a frame because it does not own a receive buffer indicating loss of data. When MISS is set, RXON is cleared and an interrupt will be generated if INEA = 1. If MISS is set while a data link is established, the MK50H25 will go into the Local Busy state and will send an RNR response frame to the remote station. Upon clearing MISS the MK50H25 will send a RR response frame. MISS is READ/CLEAR ONLY and is set by MK50H25 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
05	ROR	RECEIVER OVERRUN indicates that the Receiver FIFO was full when the receiver was ready to input data to the Receiver FIFO. When ROR occurs, the receive FIFO will be flushed and the buffer(s) containing any part of the frame already received will be re-used by the next incomming frame. Therefore, the frame being received is lost, but is typically recoverable through the protocol used. When ROR is set, an interrupt is generated if INEA = 1. ROR is READ/CLEAR ONLY and is set by MK50H25 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
04	TUR	TRANSMITTER UNDERRUN indicates that the MK50H25 has aborted a frame since data was late from memory. This condition is reached when the transmitter and transmitter FIFO both become empty while transmitting a frame. The frame in transmission at the time will be aborted. When TUR is set, an interrupt is generated if INEA = 1. TUR is READ/CLEAR ONLY and is set by MK50H25 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
03	PINT	PRIMITIVE INTERRUPT is set after the chip updates the primitive register to issue a provider primitive. When PINT is set, an interrupt is generated if INEA =1. PINT is READ/CLEAR ONLY and is set by MK50H25 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
02	TINT	TRANSMITTER INTERRUPT is set after the chip updates an entry in the Transmit Descriptor Ring. This occurrs when a transmitted I frame has been acknowledged by the remote station. When transmitting UI frames, or in Transparent Mode, TINT is set upon completing transmission of the frame. When TINT is set, an interrupt is generated if INEA = 1. TINT is READ/CLEAR ONLY and is set by the MK50H25 and

		cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
01	RINT	RECEIVER INTERRUPT is set after the MK50H25 updates an entry in the Receive Descriptor Ring. This occurs when the MK50H25 has successfuly received an I, UI, or FRMR frame, and any good frame in Transparent Mode. When RINT is set, an interrupt is generated if INEA = 1. RINT is READ/CLEAR ONLY and is set by the MK50H25 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a Stop primitive.
00	0	This bit is READ ONLY and will always read as a zero.

4.1.2.2 Control and Status Register 1 (CSR1)

RAP <3:1> = 1

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
UERR	UAV	UPARM <1:0>		UPRIM < 3:0 >				PLOST	PAV	PPARM	1:0	PPRIM < 3:0 >			

BIT	NAME	DESCRIPTION
15	UERR	USER PRIMITIVE ERROR is set by the MK50H25 when a primitive is issued by the user which is in conflict with the current status of the chip. UERR is READ/CLEAR ONLY and is set by MK50H25 and cleared by writing a "1" into the bit. Writing a "0" in this bit has no effect. It is also cleared by Bus RESET.
14	UAV	USER PRIMITIVE AVAILABLE is set by the user when a primitive is written into UPRIM. It is cleared by the MK50H25 after the primitive has been processed. This bit is also cleared by a Bus RESET.
13	UPARM	USER PARAMETER is written by the host in conjunction with the user primitives in UPRIM. This User Parameter field provides information to the MK50H25 concerning the corresponding user primitive. For connect and reset primitives this field determines what the MK50H25 will do with frames in the transmit descriptor ring which have previously been sent but not acknowledged. If UPARM = 0, these frames will be resent when the new link is established. If UPARM = 1, these frames will be discarded and their OWNA bits cleared, releasing ownership back to the host. For other primitives UPARM = 0 unless otherwise indicated.
12:08	UPRIM	USER PRIMITIVE is written by the user, in conjunction with setting UAV, to control the MK50H25 link procedures. The following primitives are available:
	0	Stop: Causes MK50H25 to enter the Stopped mode or phase. All DMA activity ceases, the transmitter transmits all ones, and all received data is ignored. A Stop primitive issued during transmission of a frame will cause the frame to be aborted as the Transmitter outputs 1's. A Stop primitive issued with UPARM=1 will cause a software Reset of the MK50H25 (equivalent to asserting the RESET pin).
	1	Start: Instructs the MK50H25 to exit the Stopped Mode and enter the Disconnected phase, if UPARM = 0. The descriptor Rings are reset. The transmitter begis to output flags. If issued with UPARM = 1 the MK50H25 will directly enter the Information Transfer phase (link connected). Valid only in Stopped Mode or Transparent Mode.

		2	Init: Instructs the MK50H25 to read the Initialization Block from memory. Valid only in the Stopped mode or phase. This should be performed prior to the Start primitive after a bus reset or power-up.
		3	Trans: Instructs MK50H25 to enter the Transparent Mode of operation. Data frames are transmitted and received out of the descriptor rings with no Address and Control fields prepended to the frames. If the PROM bit is set in the Protocol Parameters register, then no address filtering is performed on received frames. Transparent Mode may be exited with a Stop primitive or by a bus reset. Exiting from Transparent Mode to the information transfer phase (link connected) is possible by issuing a Start primitive with UPARM = 1, or to the Disconnected phase by issuing Start with UPARM = 0.
		4	Status Request: Instructs the MK50H25 to write the current chip status into the STATUS BUFFER. Valid in all states, but only after the Init primitive has been previously issued.
		5	Self-Test Request: Instructs the MK50H25 to perform the built in internal self test. Valid only in the Stopped phase. A Self Test primitive issued with UPARM=3 will cause the device to identify itself by returning a Provider primitive of 5 (or 7 for the MK50H27, etc). See section 4.4.12 for the self test procedure.
		6	Connect Request: Instructs the MK50H25 to attempt to establish a logical link with the remote station. Valid only in Disconnected phase .
		7	Connect Response: Indicates willingness to establish a logical link with the remote station. Valid only in Disconnected phase after receiving a Connect Indication primitive.
		8	Reset Request: If a logical link has been established, it instructs the MK50H25 to attempt to reset the current link with the remote station. In Transparent Mode or Disconnected Phase, it instructs the MK50H25 to start the T1 timer (to be used as a general purpose timer).
		9	Reset Response: If a logical link has been established, it indicates willingness to reset the current logical link with remote station. Valid only after receiving Reset Indication primitive. In Transparent Mode or Disconnected Phase, it instructs the MK50H25 to stop the T1 timer.
		10	XID Request: Instructs the MK50H25 to send a XID frame to the remote station. Data in the XID/Test Transmit buffer is used for the Data Field. Invalid in Stopped Mode.
		11	XID Response: Instructs the MK50H25 to send an XID response frame to the remote station. Data in the XID/TEST Transmit buffer is used for the data field. Valid only after receiving an XID Indication primitive.
		12	TEST Request: Instructs MK50H25 to send a TEST command to the remote station. Data in the XID/TEST Transmit buffer is used for the data field. Invalid in Stopped mode.
		13	TEST Response: Instructs MK50H25 to send a TEST response frame to the remote station. Data in XID/TEST Transmit buffer is used for the data field. Valid only after receiving TEST Indication primitive.
		14	Disconnect Request: Instructs the MK50H25 to disconnect the current logical link and enter the Normal Disconnected phase. If the link is currently disconnected, issuing Disconnect Request with UPARM=0 will cause a DM/F=0 frame to be sent; issuing it with UPARM=1 will cause a DISC/P=0 frame to be sent.
07	PLOST		PROVIDER PRIMITIVE LOST is set by the MK50H25 when a provider primitive cannot be issued because the PAV bit is still set from the previous provider primitive. PLOST is cleared when PAV is cleared or by a Bus RESET. Writing to this bit has no effect.
06	PAV		PROVIDER PRIMITIVE AVAILABLE is set by the MK50H25 when a new provider primitive has been placed in PPRIM. PAV is READ/CLEAR

ONLY and is set by the chip and cleared by writing a "1" to the bit or by Bus RESET. Under normal operation the host should clear the PAV bit after PPRIM is read.

05:04 PPARM — PROVIDER PARAMETER provides additional information about the reason for the receipt of certain primitives. The following table shows the parameters for the applicable provider primitives. This field is undefined for other provider primitives.

PPRIM / PPARM	Disconnect Indication	Disconnect Confirmation	Reset Indication	Error Indication	Remote Busy Indication
0	Remotely Initiated	UA or DM F=1 Received	Remotely Initiated	Unsolicited DM/F=0 Rcvd	Remote Busy RNR Received
1	SABM Timeout	DISC Timeout		Timer Recovery Timeout	Remote Un-Busy RR or REJ Rcvd.
2	FRMR Sent the DISC or DM Rcvd.		FRMR Sent then SABM/E Received	FRMR Received	
3	T3 Timeout	T3 Timeout		Unsolicited Ua or F bit Received	

03:00 PPRIM — PROVIDER PRIMITIVE is written by the MK50H25, in conjunction with with setting the PAV bit, to inform the user of link control conditions. Valid Provider Primitives are as follows:

2 — Init Confirmation: Indicates MK50H25 Init Block reading has completed.

3 — Watchdog Timer Expiry Indication: Indicates expiration of TCLK or RCLK watchdog timer as determined by the value of PPARM. (PPARM=1indicates TCLK, PPARM=2 indicates RCLK If PLOST is set it indicates both RCLK and TCLK watchdog timer expiry). Issued only if enabled.

4 — Error Indication: Indicates an Error condition has occurred during the Information Transfer phase that requires instruction by the Host for recovery. See the PPARM table for specific error conditions. Appropriate Host responses are Connect Response or Disconnect Request.

5 — Remote Busy Indication: Indicates change in the Remote Busy status of the MK50H25. See PPARM table for specific conditions. This primitive is only generated if RBSY (bit 11 of IADR+16) is set = 1.

6 — Connect Indication: Indicates attempt by the Primary station to establish a logical link (SABM received). Appropriate user responses are Connect Response or Disconnect Request.

7 — Connect Confirmation: Indicates sucess of a previous Connect Request by the user. A logical link is now established.

8 — Reset Indication: If a logical link has been established, it indicates an attempt by the Primary station to reset the current logical link (SABM received). Appropriate user responses are Reset Response or Disconnect Request. In Transparent Mode or Disconnected Phase, it indicates expiry of timer T1.

9 — Reset Confirmation: Indicates sucess of a previous Reset Request by the user. The current logical link has now been reset.

10 — XID Indication: Indicates the receipt of an XID command. The data field

of the XID command is located in the XID/TEST Receive buffer. Valid only if XIDE bit in CSR2 is set.

11 XID Confirmation: Indicates the receipt of an XID response. The data field of the XID command is located in the XID/TEST Receive buffer. Valid only if XIDE bit in CSR2 is set.

12 TEST Indication: Indicates the receipt of TEST command. The data field of the TEST command is located in the XID/TEST Receive buffer.

13 TEST Confirmation: Indicates the receipt of an TEST response. The data field of the XID command is located in the XID/TEST Receive buffer. Valid only if XIDE bit in CSR2 is set.

14 Disconnect Indication: Indicates request by the remote station to disconnect the current logical link (DISC received), or the refusal of a previous Connect or Reset Request. The chip is now in the Disconnected phase.

15 Disconnect Confirmation: Indicates the completion of a previously requested link disconnection.

4.1.2.3 Control and Status Register 2 (CSR2)

RAP<3:1> = 2

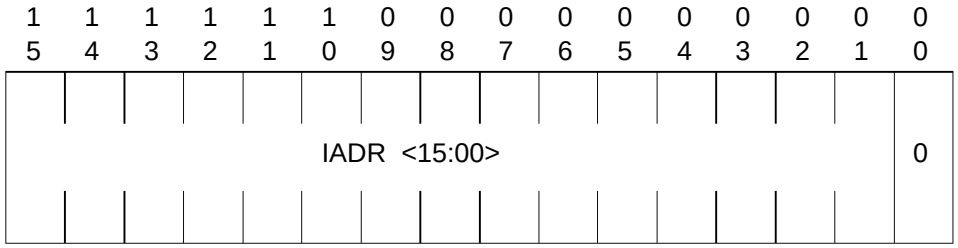
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CYCLE	EIBEN	FRMRD	T203E	X75E	PROM	UIE	XIDE	IADR<23:16>							

BIT	NAME	DESCRIPTION
15	CYCLE	Setting this bit selects a shorter DMA cycle (5 vs 6 SYSCLKs for bursting or 5 vs 7 SYSCLKs for single DMA). See Figures 7a and 8a for details.
14	EIBEN	Extended Initialization Block Enable. Setting this bit will cause the MK50H25 to use an extended Initialization Block which uses all of IADR+08 as a 16-bit scaler, moves N2 to the upper byte of IADR+40, and extends the Init Block past IADR+55. This bit is READ/WRITE.
13	FRMRD	Setting this bit disables the sending of FRMR frames (used for LAPD applications); otherwise the MK50H25 behaves as specified for X.25. This bit is READ/WRITE.
12	T203E	If this bit is set, the T3 timer is reconfigured to behave as specified for LAPD T203 timer; otherwise it behaves as specified for X.25. The operation of the T203 timer is that it expires after T203 time of not having received any type of frame, and causes a RR/P=1 polling (Timer Recovery) procedure to begin. This bit is READ/WRITE.
11	X75E	X.75 mode of protocol operation is enabled if this bit is set to 1; otherwise X.25 mode is enabled. This bit is READ/WRITE.
10	PROM	Address filtering is disabled for Transparent Mode if this bit is set. All uncorrupted incomming frames are placed in the Receive Descriptor Ring. This bit is READ/WRITE and should be set only in Transparent Mode.
9	UIE	UI frames are recognized only if this bit is set. If UIE=0 all received UI frames will not be recognized. This bit is READ/WRITE.
8	XIDE	XID frames are recognized only if this bit is set. If XIDE=0 all received XID frames will not be recognized. This bit is READ/WRITE.

07:00	IADR	The high order 8 bits of the address of the first word (lowest address) in the Initialization Block. IADR must be written by the Host prior to issuing an INIT primitive.

4.1.2.4 Control and Status Register 3 (CSR3)

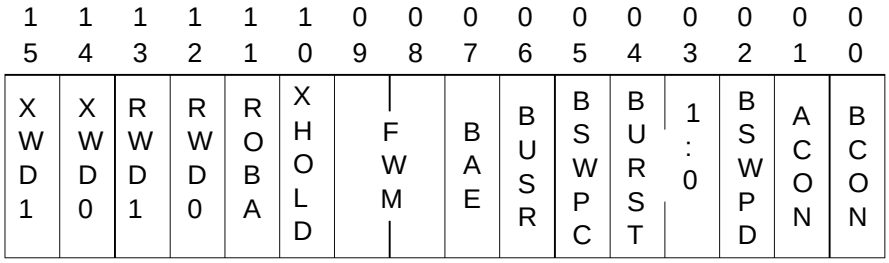
RAP<3:1> = 3



BIT	NAME	DESCRIPTION
15:00	IADR	The low order 16 bits of the address of the first word (lowest address) in the Initialization Block. Must be written by the Host prior to issuing an INIT primitive. The Initialization block must begin on an even byte boundary.

4.1.2.5 Control and Status Register 4 (CSR4)

CSR4 allows redefinition of the bus master interface.
RAP<3:1> = 4



BIT	NAME	DESCRIPTION
15:12	XWD0/1, RWD0/1	These bits enable and determine the timer values for the Transmit and Receive Watchdog Timers. These timers are independently programmable and are reset by any transition on the TCLK and RCLK pins respectively. The Watchdog timers will expire after approximately Wn SYSCLK cycles (if not reset by transition on TCLK / RCLK pins) and Provider Primitive 3 will be issued. The following table shows the selections for Wn:

XWD1/RWD1	XWD0/RWD0	Wn
0	0	Disabled
0	1	2^{18}
1	0	2^{19}
1	1	2^{20}

11	ROBA	Setting this bit will cause the MK50H25 to put the first byte of received data into both the upper and lower bytes of the receive buffer to effectively cause the Receive data to be Odd-Byte Aligned. This feature is particularly useful for extraction of odd-byte Level 3 headers from received frames leaving the remaining data even byte aligned.
10	XHOLD	Setting this bit enables the Transmit FIFO Hold-off mechansim of the MK50H25. The Transmit FIFO Hold-off watermark is selected along with the FIFO watermark so as to avoid possible conflicts.

09:08 FWM

These bits define the FIFO watermarks. FIFO watermarks prevent the MK50H25 from performing DMA transfers to/from the data buffers until the FIFOs contain a minimum amount of data or space for data. For receive, data will only be transferred to the buffers after the FIFO has at least N 16-bit words or end of frame has been reached. Conversely, for transmit, data will only be transferred from the data buffers when the transmit FIFO has room for at least N words of data. The Transmit Threshold FIFO Watermark is also defined by these bits. If enabled by setting XHOLD=1, the transmitter will be held-off from transmitting a new frame until the transmit FIFO has at least N words of data, or the entire frame has been placed in the FIFO. The N is defined as follows:

FWM<1:0>	FWM_N	XHOLD_N
11	Not Allowed	Not Allowed
10*	9 words	19 words
01	17 words	11 words
00	25 words	3 words

* Suggested setting

07 BAE

Bus Address Enable: If BAE is set, the A23-A20 pins are driven by the MK50H25 constantly providing the ability to use A23-A20 for memory bus selection. If clear, A23-A20 behave identically to A19- A16.

06 BUSR

If this bit is set, pin 15 becomes input $\overline{\text{BUSREL}}$. If this bit is clear then pin 15 is either BM0 or BYTE depending on bit 00. For more information see the description for pin 15 in this document. BUSR is READ/WRITE and cleared on bus Reset.

05 BSWPC

This bit determines the byte ordering of all "non-data" DMA transfers. This transfers refers to any DMA transfers that access memory other than the data buffers themselves. This includes the Initialization Block, Descriptors, and Status Buffer. It has no effect on data DMA transfers. BSWPC allows the MK50H25 to operate with memory organizations that have bits 07:00 at even addresses and with bits 15:08 at odd addressses or vice versa. BSWPC is Read/Write and cleared by BUS RESET.

With BSWPC = 1:

Address				Address			
XX0	0	. . .	7	XX1	8	. . .	15

With BSWPC = 0:

Address				Address			
XX0	8	. . .	15	XX1	0	. . .	7

04:03 BURST

This field determines the maximum number of data transfers performed each time control of the host bus is obtained. BURST is READ/WRITE and cleared on bus Reset.

BURST <1:0>	8 bit mode	16 bit mode
00	2 bytes	1 words
10*	16 bytes	8 words
01	unlimited	unlimited

*** Suggested setting**

02 BSWPD

This bit determines the byte ordering of all data DMA transfers. Data transfers are those to or from a data buffer. BSWPD has no effect on non-data transfers. The effect of BSWPD on data transfers is the same as that of BSWPC on non-data transfers (see above). For most applications, this bit should be set.

01 ACON

ALE CONTROL defines the assertive state of pin 18 when the MK50H25 is a Bus Master. ACON is READ/ WRITE and cleared by Bus RESET.

ACON	PIN18	NAME
0	ASSERTED HIGH	ALE
1	ASSERTED LOW	$\overline{AS}$

00 BCON

BYTE CONTROL redefines the Byte Mask and Hold I/O pins. BCON is READ/WRITE and cleared by Bus RESET.

BCON	PIN16	PIN15	PIN17
0	$\overline{BM1}$	$\overline{BM0}$	HOLD
1	$\overline{BUSAKO}$	BYTE	$\overline{BUSRQ}$

4.1.2.6 Control and Status Register 5 (CSR5)

CSR5 facilitates control and monitoring of modem controls.
RAP<3:1> = 5

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	XEDGE	RTSEN	DTRD	DSRD	DTR	DSR

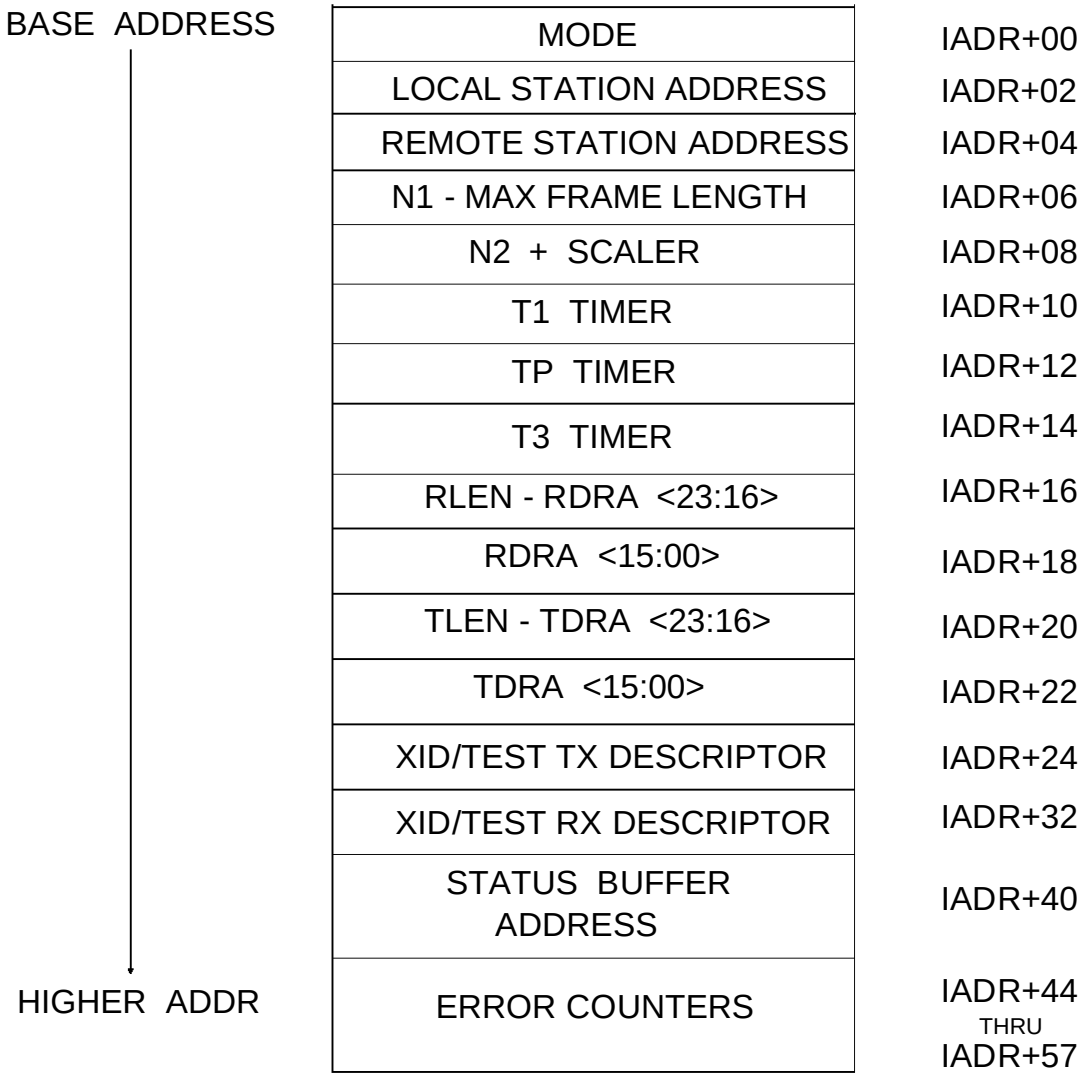
BIT	NAME	DESCRIPTION
15:06	0	Reserved, must be written as zeroes.
5	XEDGE	Setting this bit causes the TD output to change on the rising edge of TCLK rather than on the falling edge as indicated in the description of pin 25. This may be useful at high TCLK rates where internal delays may cause application required TD to TCLK setup times to otherwise be violated.
4	RTSEN	RTS/CTS ENABLE is a READ/WRITE bit used to configure pins 26 and 30. If this bit is set, pin 26 becomes $\overline{RTS}$ and pin 30 becomes CTS. RTS is driven low whenever the MK50H25 has data to transmit and is kept low during transmission. RTS will be driven high after the closing flag of a signal unit is transmited if either no other frames are in the FIFO or if the minimum signal unit spacing is higher than 2 (see Mode Register). The MK50H25 will not begin transmission and TD will remain HIGH if CTS is high. If RTSEN = 0 then pins 26 and 30 become programmable I/O pins DTR and DSR. The direction and behavior of DSR and DTR are controlled by the following bits.
3	DTRD	DTR DIRECTION is a READ/WRITE bit used to control the direction of the DTR/RTS pin. If DTRD = 0, the DTR/RTS pin becomes an input pin and the DTR bit reflects the current value of the pin; if DTRD = 1, the DTR/RTS pin is an output pin controlled by the DTR bit below.
2	DSRD	DSR DIRECTION is a READ/WRITE bit used to control the direction of the DSR/CTS pin. If DSRD = 0, the DSR/CTS pin becomes an input pin and the DSR bit reflects the current value of the pin; if DSRD = 1, the DSR/CTS pin is an output pin controlled by the DSR bit below.
1	DTR	DATA TERMINAL READY is used to control or observe the DTR I/O pin depending on the value of DTRD. If DTRD = 0, this bit becomes READ ONLY and always equals the current value of the DTR/RTS pin. If DTRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DTR/RTS pin.

0	DSR	DATA SET READY is used to control or observe the DSR I/O pin depending on the value of DSRD. If DSRD = 0, this bit becomes READ ONLY and always equals the current value of the DSR/CTS pin. If DSRD = 1 this bit becomes READ/WRITE and any value written to this bit appears on the DSR/CTS pin.

4.2 Initialization Block

MK50H25 initialization includes the reading of the Initialization Block in the off-chip memory to obtain the operating parameters. The Initialization Block is defined below. Upon receiving an Init primitive, portions of the Initialization block are read by the MK50H25. The remainder of the Initialization block will be read as needed by the MK50H25.

Figure 8: Initialization



4.2.1 Mode Register

The Mode Register allows alteration of the MK50H25's operating parameters.

IADR + 00

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MFS <4:0>					EXTCF	EXTAF	DACE	EXTC	EXTA	DRFCS	DTFCS	FCSS	LBACK <2:0>		

BIT	NAME	DESCRIPTION
15:11	MFS<4:0>	Minimum Frame Spacing defines the minimum number of flag sequences transmitted between adjacent frames transmitted by the MK50H25. This only affects frames transmitted by the MK50H25 and does not restrict the spacing of the frames received by the MK50H25. When using RTS/CTS control this field defines the number of flags transmitted at the beginning of the frame after CTS is driven low (minus one for the trailing flag). See the following table for encoding of this field.

NUMBER OF FLAGS	MFS<4:0>	NUMBER OF FLAGS	MFS<4:0>
1	1	32	28
2	0	34	24
4	2	36	17
6	4	38	3
8	9	40	6
10	18	42	13
12	5	44	27
14	11	46	23
16	22	48	14
18	12	50	29
20	25	52	26
22	19	54	21
24	7	56	10
26	15	58	20
28	31	60	8
30	30	62	16

10	EXTCF	Extended Control Force. If set along with EXTC, the receiver will assume the control field to be two octets long regardless of the first two bits of the control field. See EXTC below.
09	EXTAF	Extended Address Force. If set along with EXTA, the receiver will assume the address to be two otets long regardless of the first bit of the address. See EXTA below.
08	DACE	Address and control field extraction are disabled when DACE is set Address and control fields are treated as data and placed in memory as such. DACE must be written with "1" for normal transparent data transfer operation, but can be set to "0" for doing address and control field filtering.
07	EXTC	Extended Control Field filtering is enabled when EXTC = 1 if DACE = 0 and PROM = 0 (PROM is in CSR2).
06	EXTA	Extended Address Field filtering is enabled when EXTA = 1 if DACE = 0 and PROM = 0 (PROM is in CSR2).
05	DRFCS	Disable Receiver FCS (CRC). When DRFCS = 0, the receiver will extract and check the FCS field at the end of each frame. When DRFCS = 1, the receiver continues to extract the last 16 or 32 bits of each frame,

depending on FCSS, but no check is performed to determine whether the FCS is correct. If the received frame has no FCS, then the FCSEN bit (in IADR+16) should be set so that MCNT will reflect the correct length of the received frame.

04 DTFCS — Disable Transmitter FCS. When DTFCS=0, the transmitter will generate and append the FCS to each signal unit. When DTFCS = 1, the FCS logic is disabled, and no FCS is generated with transmitted frames.

Setting DTFCS = 1 is useful in loopback testing for checking the ability of the receiver to detect an incorrect FCS.

03 FCSS — FCS Select. When FCSS = 1, a 16-bit FCS is selected otherwise a 32-bit FCS is used.

02:00 LBACK — Loopback Control puts MK50H25 into one of several loopback configurations. *(Note: If RTSEN (CSR5<04>) = 1, then* $\overline{\text{RTS}}$ (pin 26) must be connected to $\overline{\text{CTS}}$ (pin 30) for proper loopback operation.)

LBACK	DESCRIPTION
0	Normal operation. No loopback.
4	Simple loopback. Receive data and clock are driven internally by transmit data and clock. Transmit clock must be supplied externally
5	Clockless loopback. Receive data is driven internally by transmit data. Transmit and receive clocks are driven by SYSCLK divided by 8.
6	Silent loopback. Same as simple loopback with td pin forced to all ones.
7	Silent clockless loopback. Combination of Silent and Clockless loopbacks. Receive data is driven internally by transmit data, transmit and receive clocks are driven by SYSCLK divided by 8. The TD pin is forced to all ones.

4.2.2 Station Addresses

The MK50H25 uses the values in Local and Remote Station Address fields of the Initialization Block for filtering received frames and for the address field of transmitted frames. The MK50H25 transmits commands with the Remote Station Address in the frame address field, and it transmits responses with the Local Station Address in the frame address field. The MK50H25 compares the received frame address to the Local and Remote Station Address fields. If the received frame address matches the Local Station Address field the MK50H25 will treat the received frame as a command. If the received frame address matches the Remote Station Address field the MK50H25 will treat the received frame as a response. The MK50H25 also supports the reception of frames with a global address of all 1's, if the XIDE bit (CSR2<08>) is set =1. In this case, it will treat a frame received with a global address as a comand, whether or not it is an XID/TEST frame. The MK50H25 however, will transmit a frame with a global address if all 1's have been placed in the appropriate Local/Remote Address fields prior to an Init primitive (UPRIM=2, CSR1) being issued.

4.2.3 Station Address and Control Field Filtering

The Local and Remote frame addresses may be either one or two octets according to the EXTA control bit described in the MODE register. If extended address mode filtering is selected, bit zero of the address field should be set to a zero if adherening to HDLC standards. If extended address filtering is not selected, frame adresses should be located in the lower order byte of of their respective fields. The address filtering is a one octet compare if the extended address bit, EXTA is 0 (Mode register bit 06), or follows the HDLC rules for extended addressing if EXTA is 1. Frames not matching either address are ignored.

In the MK50H25, address filtering and control field handling applies only to octet aligned frames received with good FCS. Any frame not meeting both of these conditions is discarded and the "Bad Frames Received" error counter (located at IADR + 38 of the Initialization Block) is incremented.

Extended control field filtering is also possible using the EXTC bit (Mode Register bit 07), as shown in Table 2 and Table 3. If EXTC is 0 then the C-field is one octet for all frames. If however EXTC is set to 1, the MK50H25 will look to see if either of the two least significant bits of the C-field is 0. If so, the frame is said to have an extended control field which is two octets. In addition, bits EXTAF and EXTCF (Mode Register bit 09 & 10) are useful to force extended address and control. If EXTAF is set along with EXTA, the receiver will assume the address field to be two bytes long regardless of the first bit of the address field. If EXTCF is set along with EXTC, the receiver will assume the contol field to be two bytes long regardless of the first two bits of that field.

The following table shows the MK50H25 address filtering options and handling of the received Address field.

Table 2: MK50H25 Address Filtering Options

EXTA	EXTAF	XIDE	PROM	DACE	ADDRESS FILTERING
0	**0**	**0**	**0**	**0**	Single octet filtering L&R (Local & Remote frame adresses)
X	**X**	**X**	**1**	**1**	No address filtering, all frames accepted
0	**0**	**1**	**0**	**0**	Single octet filtering L&R and global addresses
0	**X**	**X**	**X**	**1**	Not allowed
1	**0**	**0**	**0**	**0**	Double octet filtering L&R per HDLC rules
1	**0**	**0**	**0**	**1**	Double octet filtering L&R per HDLC rules
1	**1**	**0**	**0**	**0**	Double octet filtering L&R regardless of A-field LSB
0	**1**	**X**	**X**	**0**	Not allowed

NOTES:

1. PROM is defined in CSR2 bit 10. XIDE is defined in CSR2 bit 08.
2. DACE, EXTA, EXTAF, EXTC, and EXTCF are defined in the Mode register. X = Do not care.
3. DACE and PROM should be set =1 only in Transparent Mode operation.

In Transparent Mode, address filtering is supported if the PROM bit (CSR2, bit 10) is 0. In this case, frames are accepted if the received Address field matches either the Send Frame Address or the Receive Frame Address as specified in the Initialization Block. The Send and Receive addresses may be either one or two octets in length according to the EXTA control bit as described above. Frames not matching either address are ignored. Bit RADR in the Receive Message Descriptor (RMD0 <09>)indicates which of the two programmable adresses the frame matched. If address filtering is not used, these fields can just be written as zeroes.

For global adresses, the XIDE bit is valid in transparent mode, depending upon the settings of the other bits in the Mode Register, as shown in Table 3 below. If bit XIDE (CSR2, bit 08) is set to 1, then all frames with address "11111111" are accepted.

The following table shows the MK50H25 address filtering options and the way in which it handles the received Address and Control fields in Transparent Mode.

Table 3: Address and Control Field Handling By The MK50H25 Receiver In Transparent Mode

DACE	PROM	EXTA	EXTAF	EXTC	EXTCF	Address Field Handling	Control Field Handling
0	**0**	**0**	**0**	**0**	**0**	A filtered	CC -> MEM1
0	**0**	**0**	**0**	**1**	**0**	A filtered	CC or EC -> MEM1
0	**0**	**1**	**0**	**0**	**0**	A or EA filtered	CC -> MEM1
0	**0**	**1**	**1**	**0**	**0**	EA filtered	CC -> MEM1
0	**0**	**1**	**0**	**1**	**0**	A or EA filtered	CC or EC -> MEM1
0	**0**	**1**	**1**	**1**	**1**	EA filtered	EC -> MEM1
0	**1**	**0**	**0**	**0**	**0**	Not filtered, AA -> MEM1	CC -> MEM2
0	**1**	**0**	**0**	**1**	**0**	Not filtered, AA ->MEM1	CC or EC -> MEM2
0	**1**	**1**	**0**	**0**	**0**	Not filtered, AA or EA -> MEM1	CC -> MEM2
0	**1**	**1**	**1**	**0**	**0**	Not filtered, EA -> MEM1	CC -> MEM2
0	**1**	**1**	**0**	**1**	**1**	Not filtered, AA or EA -> MEM1	EC -> MEM2
1	**0**	**X**	**X**	**X**	**X**	First 2 octets always filtered	EC -> MEM1
1	**1**	**X**	**X**	**X**	**X**	Total transparent mode	All data after opening flag & before FCS -> memory

NOTES:

1. MEM1 is the first location and MEM2 is the second location where received data is loaded. MEM1 and MEM2 are each 16 bits wide.

2. C is the received, single octet, control field. CC ->MEMx means the single octet control field C is loaded into both bytes of a 16 bit memory location. Similarly, A is a single octet address field, and AA ->MEMx means the single octet address field A is loaded into both bytes of a 16 bit memory location.

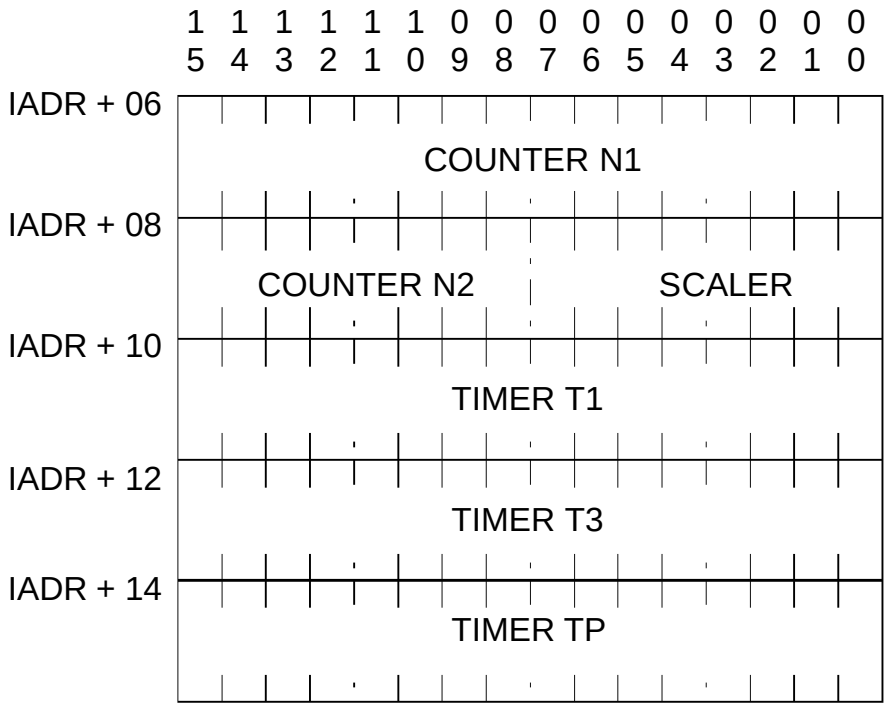
3. EC is an extended control field (2 octets). If EXTC=1 and either of the 2 LSB's of the control filed is 0, the control field is considered extended, This determines whether CC or EC ->MEMx. However, when EXTCF is set to 1, the control field is always extended

4. EA is an extended address field (2 octets). "A or EA filtered" means that one octet of the A-field is filtered if the LSB = 1, or two octets are filtered if the LSB = 0. Similarly "AA or EA -> MEM1" means that AA is loaded into memory if the LSB = 0; else, EA is loaded. This conforms to HDLC rules for extended address. However, if EXTAF is set to 1, two octets are filtered regardless of the LSB, and EA will be loaded into memory.

5. .PROM is defined in CSR2 bit 10.

6. DACE, EXTA, EXTAF, EXTC, and EXTCF are as defined in the Mode register. X = Do not care.

4.2.4 Timer/Counters

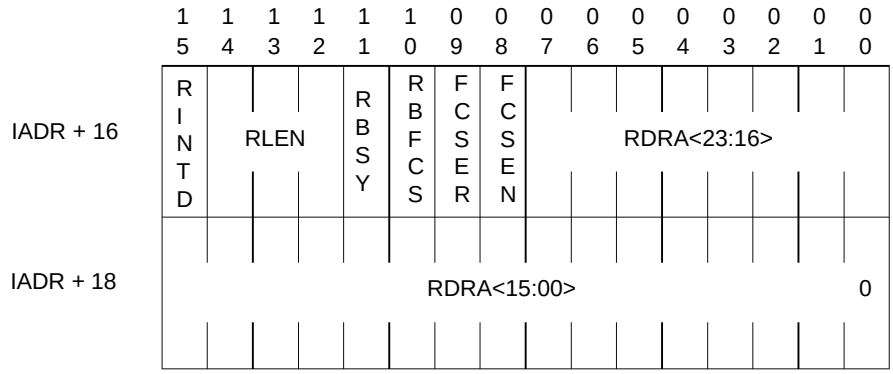


There are 5 independent counter-timers. The Host will write the value of these to the Initialization Block.

COUNTER	DESCRIPTION
N1	MAXIMUM FRAME LENGTH. This field must contain the two's complement of one less than the maximum allowable frame length, in bytes. Any frame that exceeds this count will be discarded.
N2	MAXIMUM RETRANSMISSION COUNT. This field must contain the two's complement of one less than the maximum number of retransmissions that will be made following the expiration of T1. If CSR2<14> bit EIBEN=1 then the MK50H25 will expect the value for counter N2 to be located in the upper byte of IADR + 40.
SCALER	TIMER PRESCALER. Timers T1, T3, and TP are scaled by this number. The prescaler is incremented once every 32 system clock pulses. When it reaches the timers are incremented and the prescaler is reset. This field is interpreted as two's complement of the prescaler period. If CSR2<14> bit EIBEN=1 then the MK50H25 will use the entire 16-bit value at IADR+08 as the prescaler value. This may be required to achieve long timer values when operating a high SYSCLK speeds. Note: a prescale value of 1 gives the smallest amount of scalling to the timers (64 clock pulses); zero gives the largest (8224 clock pulses if EIBEN=0, or 2,097,184 clock pulses if EIBEN=1).
T1	RETRANSMISSION TIMER. Link control frames will be retransmitted upon expiration of the T1 timer if the appropriate response is not received. This field must contain the two's complement of the period of timer T1. The scaled value of T1 should be made large enough to allow the remote station to receive the control frame and send its response.
T3/T203	LINK IDLE TIMER. The link idle timer determines the amount of link idle time necessary to consider the link disconnected. If CSR2<12> bit T203E=1 it determines the amount of link idle time or time without receiving a valid frame before it begins a RR/P=1 polling sequence to determine if the link is still connected. This field must contain the two's complement of the period of T3 or T203. T3 is disabled if CSR5<04> RTSEN = 1 or if the MK50H25 is in Transparent mode.

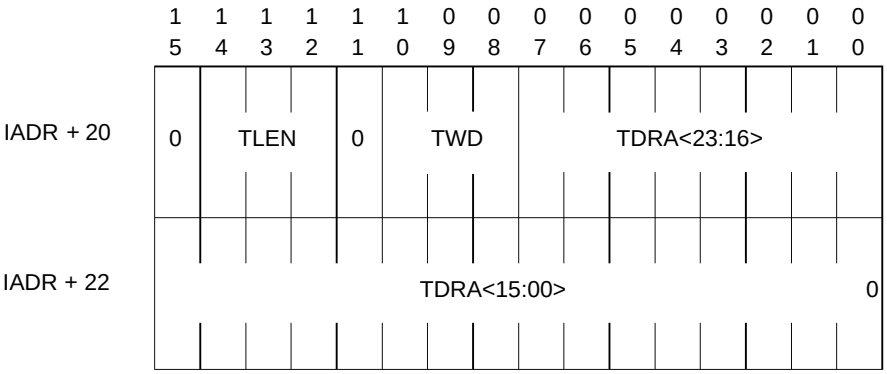
TP TRANSMIT POLLING TIMER. This scaled timer determines the length of time between polls of the Transmit Descriptor Ring to determine if there is a frame awaiting transmission (i.e. OWNA bit has been set plus other appropriate information placed in the current Transmit Descriptor). Unless TDMD (see CSR0) is set, or a frame is received (in protocol mode) on the link, no attempt is made to transmit a frame in the Transmit Descriptor Ring until TP expires. At TP expiration all frames available in the Transmit Descriptor Ring will be sent. This field must contain the two's complement of the period of timer TP.

4.2.5 Receive Descriptor Ring Pointer



BIT	NAME	DESCRIPTION
15	RINTD	RECEIVE INTERRUPT DISABLE. Setting this bit will cause no Receive Interrupt (RINT) to be generated upon the reception of any frame.
14:12	RLEN	RECEIVE RING LENGTH is the number of entries in the Receive Ring expressed as a power of two.
11	RBSY	Remote Busy indication enable. Setting this bit will enable the issuance of Remote Busy Indication primitives (PPRIM=5) upon reception of RNR or RR frame indicating a change in the busy status of the remote.
10	RBFCS	Receive frames with Bad FCS. Setting this bit causes the MK50H25 to receive frames with bad FCS when in Transparent Mode. The FRMRR bit in RMD0 will be set to indicate the received frame had a bad FCS. This bit should be set only for Transparent Mode
09	FCSER	FCSER. Setting this bit enables a separate Error Counter at IADR + 56 that will count aborted frames separately from Bad Frames Received.
08	FCSEN	Setting this bit will cause the MK50H25 to append the entire FCS of received frames to the receive data buffer, and MCNT will reflect the additional FCS bytes.
07:00/15:00	RDRA	RECEIVE DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Receive Descriptor Ring. The Receive Descriptor Address must begin on a word boundary.

4.2.6 Transmit Descriptor Ring Pointer



BIT	NAME	DESCRIPTION
15	0	Reserved, must be written as a zero.

14:12 TLEN — TRANSMIT RING LENGTH is the number of entries in the Transmit Ring expressed as a power of two.

TLEN	NUMBER OF ENTRIES	TWD	WINDOW SIZE EXTC = 0	WINDOW SIZE EXTC = 1
0	1	0	NA	1
1	2	1	1	3
2	4	2	2	7
3	8	3	3	15
4	16	4	4	31
5	32	5	5	63
6	64	6	6	127
7	128	7	7	127

11 — 0 — Reserved, must be written as a zero.

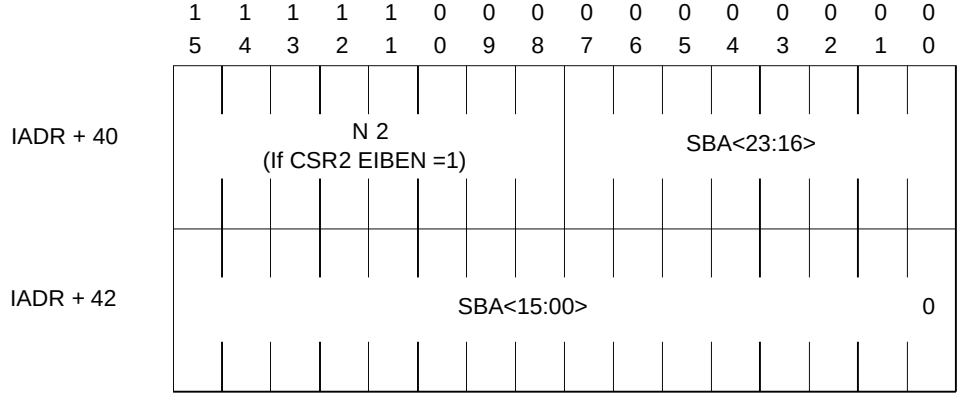
10:08 — TWD — Transmit Window is the window size of the Transmitter expressed as a power of two less one. TWD is the maximum number of I frames which may be transmitted without an acknowledgement. TWD is not allowed to be greater than 127. **For Transparent Mode set TWD = 1 or more.**

07:00/15:00 — TDRA — TRANSMIT DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Transmit Descriptor Ring. The Transmit Descriptor Ring Address must begin on a word boundary.

4.2.7 XID/TEST Descriptors

The XID/TEST Descriptors contain pointers to the buffers used to receive and transmit XID, and TEST frames, as well as buffer lengths. The exact format of these descriptors can be seen in the following Receive and Transmit Message Descriptor Entry descriptions. They are used the same as other descriptors except that no data chaining is allowed (i.e., SLF and ELF must be set to 1).

4.2.8 Status Buffer Address



BIT	NAME	DESCRIPTION
15:08	0	Reserved, must be written as zeroes.
07:00/15:00	SBA	STATUS BUFFER ADDRESS points to a 7 word status buffer into which status information is placed upon the issuance of the Status Request primitive by the HOST. The status buffer must begin on a word boundary.

4.2.9 Error Counters Seven locations in the Initialization buffer are reserved for use as error counters which the MK50H25 will increment. These counters are intended for use by the host CPU for statistical analysis. The MK50H25 will only increment the counters; it is up to the user to clear and preset them. The error counters are:

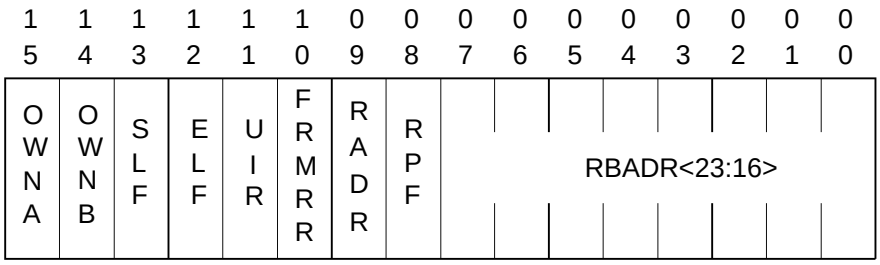
Memory Address	Error Counter
IADR + 44	Bad Frames Received - Bad FCS - Non-Octet Aligned
IADR + 46	Number of FRMR frames received.
IADR + 48	Number of T1 timeouts.
IADR + 50	Number of REJ frames received.
IADR + 52	Number of REJ frames transmitted.
IADR + 54	Frames shorter than minimum length received.
IADR + 56	Number of Aborted frames received. Enabled only if FCSER = 1
IADR + 58 thru IADR + 60	Reserved. Must be programmed as zeroes only if EIBEN = 1.

4.3 Receive and Transmit Descriptor Rings

Each descriptor ring in memory is a 4 word entry. The following is the format of the receive and transmit descriptors.

4.3.1 Receive Message Descriptor Entry

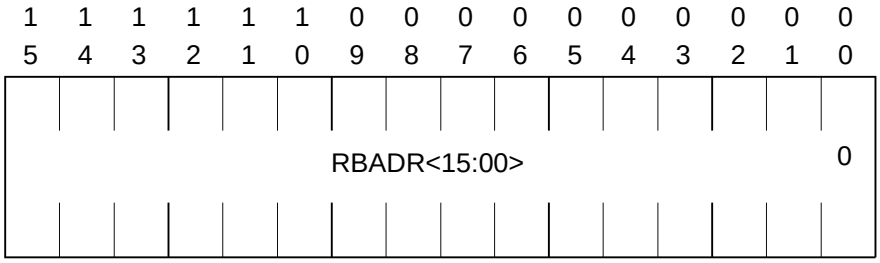
4.3.1.1 Receive Message Descriptor 0 (RMD0)



BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero either the HOST or the I/O ACCELERATION PROCESSOR owns this descriptor. When this bit is a one the MK50H25 owns this descriptor. The chip clears the OWNA bit after filling the buffer pointed to by the descriptor entry provided a valid frame has been received. The Host sets the OWNA bit after emptying the buffer. Once the MK50H25, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	OWNB	This bit determines whether the HOST or a Slave Processor or Process owns the buffer when OWNA is a zero. The MK50H25 never uses this bit.
13	SLF	Start of Long Frame indicates that this is the first buffer used by the MK50H25 for this frame. It is used for data chaining buffers. SLF is set by the MK50H25. *NOTE: A "Long Frame" is any frame which needs chaining.*
12	ELF	End of Long Frame indicates that this the last buffer used by MK50H25 for this frame. It is used for data chaining buffers. If both SLF and ELF were set, the frame would fit into one buffer and no data chaining would be required. ELF is set by the MK50H25.

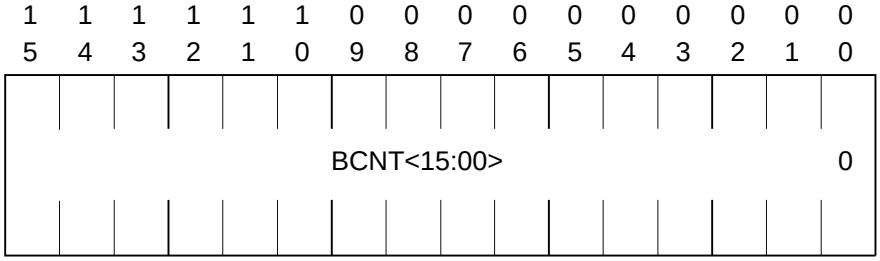
11	UIR	UI Received indicates a UI frame has been received and is in this buffer.
10	FRMRR	FRMR Received indicates the I-field of a FRMR is stored in this buffer. In Transparent mode with RBFCS=1 (IADR+16) it indicates received frame referenced by this Message Descriptor has a bad FCS.
09	RADR	Valid only in Transparent Mode with address filtering enabled, RADR indicates which of the 2 programmable addresses the frame matched. If set, the received address field matched the value in the Local Address field of the Initialization Block. Otherwise it matched the value in the Remote Address field.
08	RPF	Valid only for UI, XID, and TEST frames. RPF equals the state of the P or F bit for the received frame.
07:00	RBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK50H25.

4.3.1.2 Receive Message Descriptor 1 (RMD1)



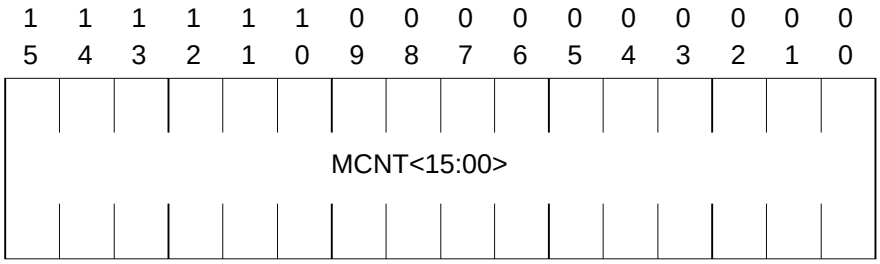
BIT	NAME	DESCRIPTION
15:01	RBADR	The low order 16 address bits of the receive buffer pointed to by this descriptor. RBADR is written by the Host CPU and unchanged by MK50H25. The receive buffers must be word aligned.

4.3.1.3 Receive Message Descriptor 2 (RMD2)



BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the length of the buffer pointed to by this descriptor expressed in two's complement. This field is written to by the Host and unchanged by MK50H25. The value of BCNT must be an even number.

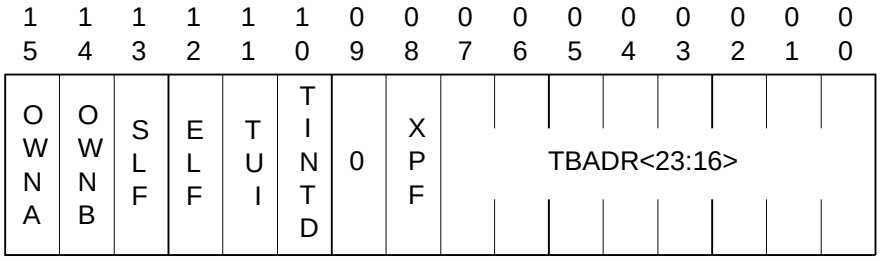
4.3.1.4 Receive Message Descriptor 3 (RMD3)



BIT	NAME	DESCRIPTION
15:00	MCNT	Message Byte Count is the length, in bytes, of the received frame MCNT is valid only when ELF is set to a one. MCNT is written by MK50H25 and read by the Host. If ELF is set to a zero the entire buffer has been utilized and the message byte count is given in BCNT above. The value of this field is expressed in two's complement. MCNT also reflects additional FCS bytes if FCSEN = 1.

4.3.2 Transmit Message Descriptor Entry

4.3.2.1 Transmit Message Descriptor 0 (TMD0)



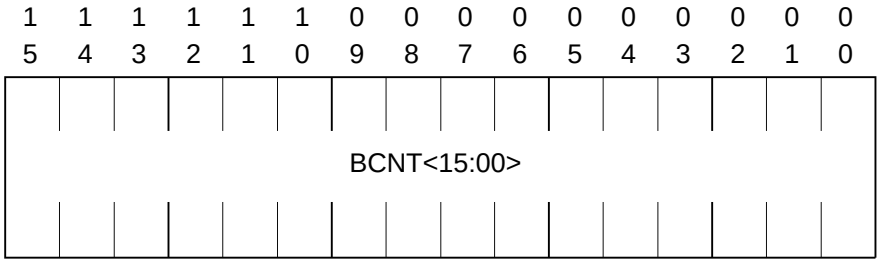
BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero either the HOST or an I /O Acceleration Processor owns this descriptor. When this bit is a one the MK50H25 owns this descriptor. The host sets the OWNA bit after filling the buffer pointed to by the descriptor entry. The MK50H25 releases the descriptor after transmitting the buffer and receiving the proper acknowledgement from the receiver. After the MK50H25, Host, or I/O Acceleration Processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	OWNB	This bit determines whether the HOST or an I /O Acceleration Processor owns the buffer when OWNA is a zero. The MK50H25 never uses this bit. This bit is provided to facilitate use of I/O Acceleration processors.
13	SLF	Start of Long Frame indicates that this is the first buffer used by the MK50H25 for this frame. It is used for data chaining buffers. SLF is set by the Host. When not chaining, SLF should be set to a one. *NOTE: A "Long Frame" is any frame which needs data chaining.*
12	ELF	End of Long Frame indicates that this is the last buffer used by the MK50H25 for this frame. It is used for data chaining buffers. If both SLF and ELF were set the frame would fit into one buffer and no data chaining would be required. ELF is set by the Host. When not chaining, ELF should be set to a one.

11	TUI	Transmit a UI frame indicates that a UI frame is to be transmitted from the transmit buffer instead of a normal I frame. **This bit must be set for anything transmitted in Transparent Mode.**
10	TINTD	Transmit Interrupt Disable. If this bit is set, no transmit interrupt is generated when ownership of this descriptor is released back to the host.
09	0	Reserved, must be written as zeroes.
08	XPF	Transmit P/F bit instructs the MK50H25 to send the corresponding frame with the respective value for the P/F bit. This bit is valid is valid only for UI, XID and TEST frames and should be written zero otherwise.
07:00	TBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK50H25.

4.3.2.2 Transmit Message Descriptor 1 (TMD1)

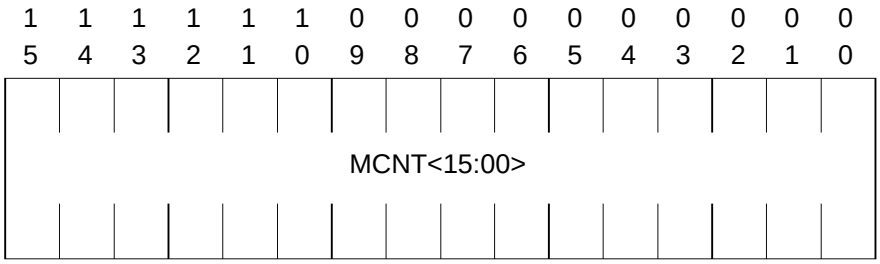
BIT	NAME	DESCRIPTION
15:00	TBADR	The Low Order 16 address bits of the buffer pointed to by this descriptor. TBADR is written by the Host and unchanged by MK50H25. The least significant bit is zero since the descriptor must be word aligned.

4.3.2.3 Transmit Message Descriptor 2 (TMD2)



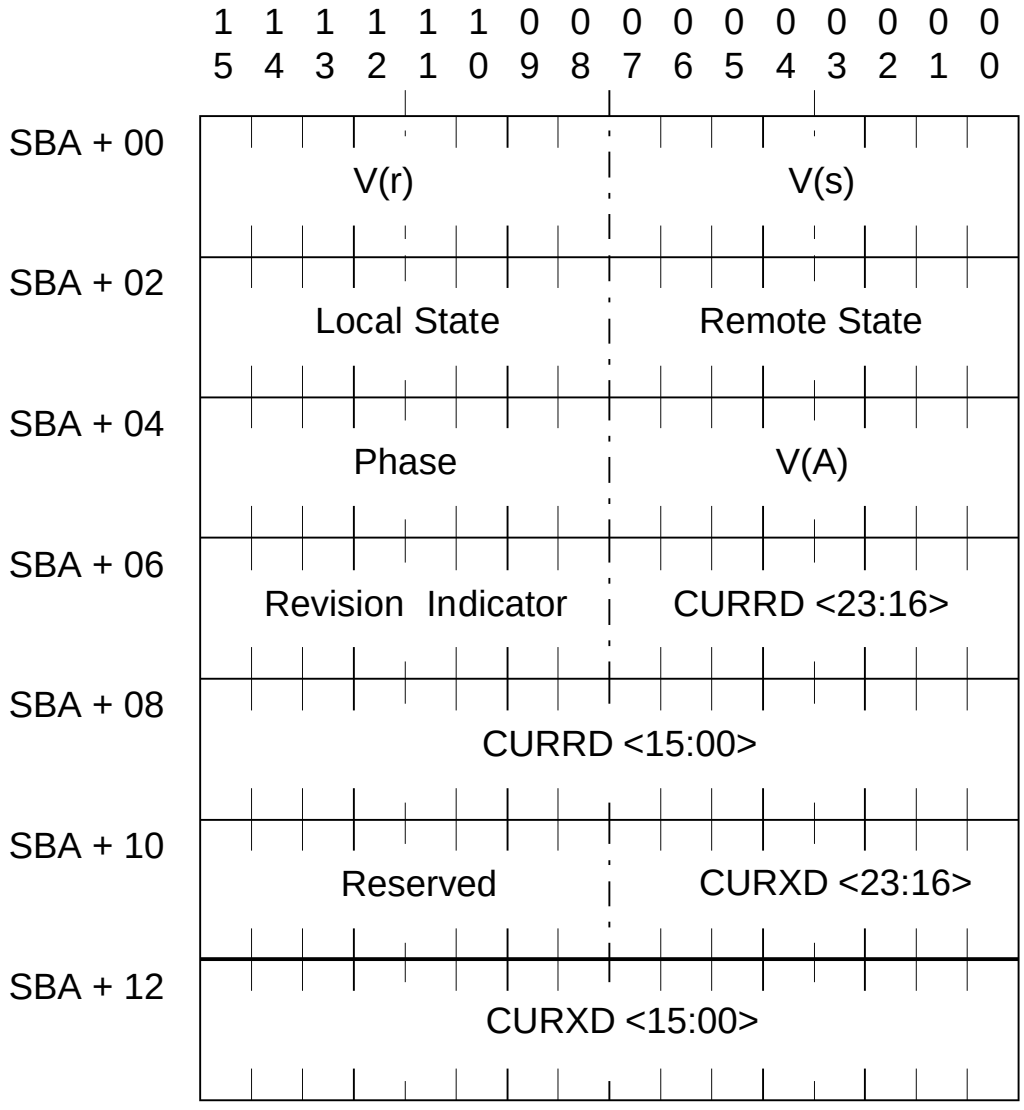
BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the usable length of the buffer pointed to by this descriptor expressed in two's complement. This field is not used by the MK50H25.

4.3.2.4 Transmit Message Descriptor 3 (TMD3)



BIT	NAME	DESCRIPTION
15:00	MCNT	Message byte count is the length, in octets, of the data contained in the corresponding buffer. The value of this field is expressed in two's complement.

4.3.3 Status Buffer



MK50H25 STATUS BUFFER

FIELD	DESCRIPTION
V(r)	Current value of the Receive Count Variable. $0 \leq V(r) \leq 7$ ($0 \leq V(r) \leq 127$ for extended control).
V(s)	Current value of the Transmit Count Variable. $0 \leq V(s) \leq 7$ ($0 \leq V(s) \leq 127$ for extended control).
V(A)	Current value of Transmit Acknowledge Count. This field contains the value of the N(r) of the most recently received S or I frame. The modulo difference between V(A) and V(s) determines the number of outstanding I frames that have not been acknowledged by the remote station.
LOCAL STATE	Indicates the current state of operation for the local (secondary) station. 0: Normal Data Transfer State 1: Local Busy State 2: REJ Sent State 3: DISC Sent State 4: Normal Disconnected State 5: SABM/E sent for link connection 6: FRMR Sent State 7: SABM/E sent for link reset 8: Error Indication issued
REMOTE STATE	Indicates the current state of operation for the remote station. 0: Remote Not Busy 1: Remote Busy
PHASE	Indicates the current phase of operation for the local station. -1: Stopped, TD is held at 1's, RD is ignored 0: Information Transfer State 1: Disconnected Phase, TD transmits flags 2: Resetting Phase 3: Transparent Data Transfer Phase 4: MERR reset phase
Revision Indicator	Indicates Firmware Revision of the device. This closely corresponds to the "REV XXX" label branded on the package of the device.
CURRD<23:0>	Current Receive Descriptor. This pointer indicates the position of the descriptor for the next receive buffer to be filled.
CURRXD<23:0>	Current Transmit Descriptor. This pointer indicates the position of the descriptor for the next transmit buffer to be transmitted.

4.4 Detailed Programming Procedures

4.4.1 Initialization (Reading of Initialization Block)

The following procedure should be followed to intialize the MK50H25:

1. Setup bus control information in CSR4.
2. Setup the Initialization Block and Desciptor Rings.
3. Load the address of the initialization block information into CSR's 2 and 3.
4. Issue the INIT primitive through CSR1 (write 4200H to CSR1) instructing the MK50H25 to read the initialization block pointed to by CSR's 2 and 3.
5. Wait for the INIT confirmation primitive (CSR1 = 0242H) from the MK50H25.

Then clear the PAV bit in CSR1 (write 0040H to CSR1).

6. Issue the Start primitive through CSR1 (write 4300H to CSR1).

Flags will now be continously transmitted.

7. Enable interrupts in CSR0 if desired.

4.4.2 Active Link Setup

The following procedure should be followed to actively establish a link.

1. Issue Connect Request primitive (UPRIM=6) through CSR1. The MK50H25 will attempt to establish a logical link. It does this by sending a SABM/P=1 frame, and repeats sending it at T1 timer intervals until a response is received or N2 have been sent (in which case it would issue PPRIM=14 with PPARM=1).
2. Wait for a Connect Confirmation primitive (PPRIM=7) from the MK50H25 (indicating reception of UA frame in response to SABM sent).
3. If a Connect Confirmation primitive is received, a link has been established.
4. If a Disconnect Indication primitive (PPRIM=14) is received, the MK5025 has been unable to establish a link. The reason will be in the PPARM field of CSR1.

4.4.3 Passive Link Setup

The following procedure should be followed for passively establishing a link.

1. Issue a Disconnect Request primitive (UPRIM=14). If issued with UPARM=0, a DM/F=0 frame will be sent; if issued with UPARM=1, a DISC/P=0 frame will be sent to the remote station requesting link setup. This step is optional in many cases, but some networks require either a DM or DISC be sent to initiate passive link setup.
2. Wait for a Connect Indication primitive (PPRIM=6) from the MK50H25.
3. If a Connect Indication primitive is received (indicating SABM frame has been received), issue a Connect Response primitive to indicate willingness to establish the link (causes MK50H25 to respond with a UA frame). The link is now established.
4. If no Connect Indication primitive is received, the remote station is not trying to establish a link.

4.4.4 Refusing Link Setup

The following procedure should be followed when refusing link establishment.

1. A Connect Indication primitive received indicates a request by the remote station to establish a link.
2. Issue a Disconnect Request primitive to refuse to establish the link (causes MK50H25 to respond with a DM or DISC frame depending on value of UPARM).

4.4.5 Sending Data

Use the following procedure to send a frame:

1. Wait for the OWNA bit of the current transmit descriptor to be cleared, if it is not already.
2. Fill the buffer associated with the current transmit descriptor with the data to be sent, or set the descriptor buffer address to any already filled buffer.
3. Repeat steps 1 & 2 for next buffer if chaining is necessary, setting SLF, ELF and MCNT appropriately.
4. Set the OWNA bit for each descriptor used.
5. Go on to next descriptor. The OWNA bits will be cleared when data has been sent successfully and acknowledged. In Transparent Mode, OWNA bits are cleared immediately after frame transmission.

4.4.6 Receiving Data

The following procedure should be followed when receiving a frame:

1. Make sure the OWNA bit of the current receive descriptor is clear.
2. Read data out of the buffer associated with the current receive descriptor.
3. Set the OWNA bit of the current receive descriptor.
4. If the ELF bit of the current receive descriptor is clear, then go on to the next descriptor and repeat the above steps appending data from each buffer until a descriptor with the ELF bit set is reached.

4.4.7 Link Disconnect

The following procedure should be followed to disconnect an established link.

1. Issue the Disconnect Request primitive to the MK50H25.
2. A Disconnect Confirmation primitive (PPRIM=15) will be issued after successful disconnection, and the MK50H25 will go into Normal Disconnected state.

4.4.8 Link Reset

The following procedure should be followed to reset an established link.

1. Issue a Reset Request primitive (UPRIM=8).
2. Wait for a Reset Confirmation primitive (PPRIM=9) from the MK50H25 (indicating reception of UA frame in response to SABM sent).
3. If a Reset Confirmation primitive is received, a link has been reset.
4. If a Disconnect Indication primitive (PPRIM=14) is received, the MK5025 was unable to reset the link. The reason will be in the PPARM field of CSR1. Link connection procedures now must be performed to re-establish the link.

4.4.9 Receiving Link Reset

The following procedure should be followed when receiving a request for link reset:

1. A Reset Indication primitive (PPRIM=8) will be received from the MK50H25 indicating the remote station has requested a resetting of the link.
2. If able to reset, issue a Reset Response primitive (UPRIM=9) to indicate willingness to reset the link.
3. If unable to reset, issue a Disconnect Request primitive (UPRIM=14) to disconnect the link.

4.4.10 Receiving FRMR Frame

The following procedure should be followed when receiving a FRMR frame:

1. An Error Indication primitive (PPRIM=4) will be received from the MK50H25 indicating an error condition. PPARM=2 will indicate a FRMR has been received. The I-field of the FRMR has been placed in the receive buffer pointed to by the next available Receive Descriptor.
2. If able to reset the link, issue a Reset Response primitive (UPRIM=9) and wait for either a Reset Indication or a Disconnect Indication as described previously for Link Reset.
3. If unable to reset, issue a Disconnect Request primitive (UPRIM=14) to disconnect the link. Link connection procedures now must be performed to re-establish the link.

4.4.11 Exchanging Identification

The following procedure should be followed to exchange identification with the remote station:

1. The XIDE bit in CSR2 must be set prior to any identification exchange.
2. Place appropriate identification information in the XID/TEST Transmit buffer.
3. Issue an XID Request primitive (UPRIM=10)
4. If an XID Confirmation primitive (PPRIM=11) is received, the identification exchange has been performed, and the remote response is located in the XID/TEST Receive buffer.

4.4.12 Receiving XID/TEST Frames

The following procedure should be performed when receiving XID/TEST frames:

1. A XID Indication primitive (PPRIM=10) or TEST Indication Primitive (PPRIM=12) will be received from the MK50H25 to indicate the reception of a XID or TEST frame. The information field of the received XID or TEST frame will be located in the XID/TEST receive buffer.
2. To respond, place the appropriate information in the XID/TEST transmit buffer and issue a XID/TEST Response Primitive (UPRIM=11/13).
3. To refuse, issue a Disconnect Request primitive (UPRIM=14).

NOTE: A XID or TEST Indication primitive will only be issued if the XIDE bit is set in CSR2. Otherwise all XID/TEST frames will automatically be refused and not recognized.

4.4.13 Disabling the MK50H25

The following procedure should be followed to disable the MK50H25:

1. Issue the STOP primitive through CSR1. This will disable the MK50H25 from receiving or transmitting. The TD pin will be held high while the MK50H25 is in the Stopped mode. The STOP bit in CSR0 will be set and interrupts will be disabled. If reception or transmission of a frame is in progress, then received data may be lost, and the transmitted frame will be aborted.

4.4.14 Re-enabling the MK50H25

The same procedure should be followed for re-enabling the MK50H25 as was used to initalize upon power up. If the Initialization Block and the hardware configuration have not changed, then steps 1,2,3, 4 and 5 of the intialization sequence may be omitted.

4.4.15 MK50H25 Internal Self Test

The MK50H25 contains an easy to use internal self test designed to test, with a high fault coverage, all of the major blocks of the device except the DMA controller. It is suggested that a loopback test also be performed to more completely test the DMA controller.

The following procedure should be followed to execute the internal self test:

1. Reset the device using the $\overline{\text{RESET}}$ pin.
2. Set bit 04 of CSR4.
3. Issue a Self Test Request (UPRIM=5) through CSR1.
4. Poll CSR1, waiting for the PAV bit in CSR1 to be set by the MK50H25.
5. After the PAV bit is set, read CSR1. If bit 04 is clear, the self test passed. If bit 04 is set, it failed. The success or failure of the test is futher indicated in the PPRIM field as follows:

PPRIM	RESULT
0	Passed self test.
1	Failed the reset test of the self test.
2	Failed the self test in the micro controller RAM.
3	Failed the self test in the ALU.
4	Failed the self test in the timers.
5	Failed the self test in the transmitter and/or receiver.
6	Failed the self test in the CSR's and/or bus master.
Otherwise	Failed device.

6. If the PAV bit is not set within 75 msec (SYSCLK = 10MHZ), then the MK50H25 is unable to respond to the Self Test Request and will not complete successfully.

If the self test passes, then after clearing the PAV bit it may be immediately reexecuted from step 3, otherwise re-execution should proceed from step 1.

After executing Self-Test, the MK50H25 should be reset before continuing with other testing or operation of the device. This is recommended because the Self-Test leaves some of the timers and registers in different states than after reset. To not reset the device after Self-Test may cause unexpected results in further operation of the device.

USER NOTES:

SECTION 5
ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
T_{UB}	Temperature Under Bias	-25 to +100	°C
T_{stg}	Storage Temperature	-65 to +150	°C
V_G	Voltage on any pin with respect to ground	-0.5 to V_{CC}+0.5	V
P_{tot}	Power Dissipation	0.5	W

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the above device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A=0 °C to 70 °C, V_{CC} = +5 V ±5 percent unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IL}		-0.5		+0.8	V
V_{IH}		+2.0		V_{CC}+0.5	V
V_{OL}	@ IOL = 3.2 mA			+0.5	V
V_{OH}	@ IOH= -0.4 mA	+2.4			V
I_{IL}	@ VIN = 0.4 to V_{CC}			+10	mA
I_{CC}	@ TSCT = 100 ns		50		µA

CAPACITANCE

f = 1MHz

Symbol	Parameter	Min.	Typ.	Max.	Units
C_{IN}	Capacitance on Input pins			10	pF
C_{OUT}	Capacitance on Output Pins			10	pF
C_{IO}	Capacitance on I/O pins			20	pF

AC TIMING SPECIFICATIONS

T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

MK50H25					-16	-25	-33	-16/25/33	
No	Signal	Symbol	Parameter	Test Condition	Min.	Min.	Min.	Max.	Units
1	SYSCLK	T_{SCT}	SYSCLK period		60	40	30	10000	ns
2	SYSCLK	T_{SCL}	SYSCLK low time		24	16	12		ns
3	SYSCLK	T_{SCH}	SYSCLK high time		24	16	12		ns
4	SYSCLK	T_{SCR}	Rise time of SYSCLK		0	0	0	8	ns
5	SYSCLK	T_{SCF}	Fall time of SYSCLK		0	0	0	8	ns
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ period		20	20	20		ns
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ low time		8	8	8		ns
8	$\overline{TCLK}$	T_{TCH}	$\overline{TCLK}$ high time		8	8	8		ns
9	$\overline{TCLK}$	T_{TCR}	Rise time of $\overline{TCLK}$	CL = 50 pF	0	0	0	8	ns
10	$\overline{TCLK}$	T_{TCF}	Fall time of $\overline{TCLK}$		0	0	0	8	ns
11	TD	T_{TDP}	TD data propagation delay after the falling edge of $\overline{TCLK}$	CL = 50 pF				13	ns
12	TD	T_{TDH}	TD data hold time after the falling edge of $\overline{TCLK}$		5	5	5		ns

AC TIMING SPECIFICATIONS (Continued) - MK50H25 -16
T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

					MK50H25 -16			
No	**Signal**	**Symbol**	**Parameter**	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
13	$\overline{\text{RCLK}}$	T_{RCT}	$\overline{\text{RCLK}}$ period		20			ns
14	$\overline{\text{RCLK}}$	T_{RCH}	$\overline{\text{RCLK}}$ high time		8			ns
15	$\overline{\text{RCLK}}$	T_{RCL}	$\overline{\text{RCLK}}$ low time		8			ns
16	$\overline{\text{RCLK}}$	T_{RCR}	Rise time of $\overline{\text{RCLK}}$		0		8	ns
17	$\overline{\text{RCLK}}$	T_{RCF}	Fall time of $\overline{\text{RCLK}}$		0		8	ns
18	RD	T_{RDR}	RD data rise time		0		8	ns
19	RD	T_{RDF}	RD data fall time		0		8	ns
20	RD	T_{RDH}	RD hold time after rising edge of $\overline{\text{RCLK}}$		2			ns
21	RD	T_{RDS}	RD setup time prior to rising edge of $\overline{\text{RCLK}}$		8			ns
22	ALE/$\overline{\text{DAS}}$	T_{DOFF}	Bus Master driver disable	Output Delay	0		40	ns
23	ALE/$\overline{\text{DAS}}$	T_{DON}	Bus Master driver enable after rising edge T1 SYSCLK	Output Delay	0		40	ns
24	$\overline{\text{HLDA}}$	T_{HHA}	Delay to falling edge of $\overline{\text{HLDA}}$ from falling edge of HOLD (Bus Master)		0			ns
25	$\overline{\text{HLDA}}$	T_{HLAH}	$\overline{\text{HLDA}}$ input setup time		20			ns
26	$\overline{\text{HLDA}}$	T_{HLAS}	Delay to rising edge HLDA from rising edge HOLD		20			ns
27	A	T_{XAS}	Address setup time	Output Delay			30	ns
28	A	T_{XAH}	Address hold time	Output Delay			25	ns
29	DAL	T_{AS}	Address setup time	Output Delay			35	ns
30	DAL	T_{AH}	Address hold time	Output Delay	0		25	ns
31	DAL	T_{RDAS}	Data setup time (Bus Master read)		20			ns
32	DAL	T_{RDAH}	Data hold time (Bus Master read)		10			ns
33	DAL	T_{WAH}	Address hold time (Bus Master write)	Output Delay			15	ns
34	DAL	T_{WDS}	Data setup time (Bus Master write)	Output Delay			25	ns
35	DAL	T_{WDH}	Data hold time (Bus Master write)	Output Delay			25	ns
36	DAL	T_{SRDS}	Data setup time (Bus Slave read)				25	ns
37	DAL	T_{SRDH}	Data hold time (Bus slave read)				25	ns
38	DAL	T_{SWDH}	Data hold time (Bus slave write)		10			ns
39	DAL	T_{SWDS}	Data setup time (Bus slave write)		10			ns
40	ALE	T_{ALES}	ALE setup time	Output Delay			30	ns
41	ALE	T_{ALHB}	ALE hold time (asserted to de-asserted) (DMA Burst)	Output Delay			20	ns
42	ALE	T_{ALHS}	ALE hold time (asserted to 3-State) (Single DMA cycle)	Output Delay			20	ns
43	$\overline{\text{DAS}}$	T_{DASS}	DAS setup time from falling edge of T2 SYSCLK (Bus Master)	Output Delay			25	ns
44	$\overline{\text{DAS}}$	T_{DASH}	DAS hold time from rising edge of SYSCLK (Bus Master)	Output Delay	5		15	ns
45	DALI/$\overline{\text{DALO}}$ BM)/BM1	T_{BMDE}	Bus Master driver enable (from 3-State to driven) (Bus Master)	Output Delay			25	ns
46	$\overline{\text{DALI}}$	T_{RIS}	$\overline{\text{DALI}}$ setup time (Bus Master read)	Output Delay			15	ns
47	$\overline{\text{DALI}}$	T_{RIH}	$\overline{\text{DALI}}$ hold time (Bus Master read)	Output Delay	5		25	ns
48	$\overline{\text{DALI}}$	T_{BMDD}	Bus Master driver disable (from driven to 3-State) (Bus Master)	Output Delay			20	ns

AC TIMING SPECIFICATIONS (Continued) - MK50H25 -16
T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

					MK50H25 -16			
No	**Signal**	**Symbol**	**Parameter**	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
49	$\overline{\text{DALO}}$	T_{ROS}	$\overline{\text{DALO}}$ setup time (Bus Master read)	Output Delay			30	ns
50	$\overline{\text{DALO}}$	T_{ROH}	$\overline{\text{DALO}}$ hold time (Bus Master read)	Output Delay			30	ns
52	$\overline{\text{CS}}$	T_{CSH}	$\overline{\text{CS}}$ hold time		10			ns
53	$\overline{\text{CS}}$	T_{CSS}	$\overline{\text{CS}}$ setup time		10			ns
54	ADR	T_{SAH}	ADR hold time		10			ns
55	ADR	T_{SAS}	ADR setup time		10			ns
56	$\overline{\text{DAS}}$	T_{SDAS}	$\overline{\text{DAS}}$ input setup time (Bus slave)		10			ns
57	$\overline{\text{DAS}}$	T_{SDSH}	$\overline{\text{DAS}}$ input hold time (Bus slave)		10			ns
58	$\overline{\text{READY}}$	T_{RDYS}	$\overline{\text{READY}}$ setup time (Bus slave)	Output Delay			15	ns
59	$\overline{\text{READY}}$	T_{SRYH}	$\overline{\text{READY}}$ hold time after rising edge of $\overline{\text{DAS}}$ (Bus slave read)				20	ns
60	$\overline{\text{READY}}$	T_{RSH}	$\overline{\text{READY}}$ setup time (Bus Master)		20			ns
61	$\overline{\text{READY}}$	T_{SRS}	$\overline{\text{READY}}$ hold time (Bus Master)		12			ns
62	READ	T_{REDS}	READ setup time (Bus slave)		10			ns
63	READ	T_{REDH}	READ hold time (Bus slave)		10			ns
64	$\overline{\text{HOLD}}$	T_{HLDS}	$\overline{\text{HOLD}}$ setup time (Bus Master)	Output Delay			20	ns
65	$\overline{\text{HOLD}}$	T_{HLDH}	$\overline{\text{HOLD}}$ hold time (Bus Master)	Output Delay			40	ns

AC TIMING SPECIFICATIONS (Continued) - MK50H25 -25
T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

					MK50H25 -25			
No	**Signal**	**Symbol**	**Parameter**	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
13	$\overline{RCLK}$	T_{RCT}	$\overline{RCLK}$ period		20			ns
14	$\overline{RCLK}$	T_{RCH}	$\overline{RCLK}$ high time		8			ns
15	$\overline{RCLK}$	T_{RCL}	$\overline{RCLK}$ low time		8			ns
16	$\overline{RCLK}$	T_{RCR}	Rise time of $\overline{RCLK}$		0		8	ns
17	$\overline{RCLK}$	T_{RCF}	Fall time of $\overline{RCLK}$		0		8	ns
18	RD	T_{RDR}	RD data rise time		0		8	ns
19	RD	T_{RDF}	RD data fall time		0		8	ns
20	RD	T_{RDH}	RD hold time after rising edge of $\overline{RCLK}$		2			ns
21	RD	T_{RDS}	RD setup time prior to rising edge of $\overline{RCLK}$		8			ns
22	ALE/$\overline{DAS}$	T_{DOFF}	Bus Master driver disable	Output Delay	0		20	ns
23	ALE/$\overline{DAS}$	T_{DON}	Bus Master driver enable after rising edge T1 SYSCLK	Output Delay	0		20	ns
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus Master)		0			ns
25	$\overline{HLDA}$	T_{HLAH}	$\overline{HLDA}$ input setup time		10			ns
26	$\overline{HLDA}$	T_{HLAS}	Delay to rising edge HLDA from rising edge $\overline{HOLD}$		10			ns
27	A	T_{XAS}	Address setup time	Output Delay			30	ns
28	A	T_{XAH}	Address hold time	Output Delay			20	ns
29	DAL	T_{AS}	Address setup time	Output Delay			35	ns
30	DAL	T_{AH}	Address hold time	Output Delay	0		20	ns
31	DAL	T_{RDAS}	Data setup time (Bus Master read)		15			ns
32	DAL	T_{RDAH}	Data hold time (Bus Master read)		10			ns
33	DAL	T_{WAH}	Address hold time (Bus Master write)	Output Delay			15	ns
34	DAL	T_{WDS}	Data setup time (Bus Master write)	Output Delay			25	ns
35	DAL	T_{WDH}	Data hold time (Bus Master write)	Output Delay			25	ns
36	DAL	T_{SRDS}	Data setup time (Bus Slave read)				25	ns
37	DAL	T_{SRDH}	Data hold time (Bus slave read)				25	ns
38	DAL	T_{SWDH}	Data hold time (Bus slave write)		10			ns
39	DAL	T_{SWDS}	Data setup time (Bus slave write)		10			ns
40	ALE	T_{ALES}	ALE setup time	Output Delay			30	ns
41	ALE	T_{ALHB}	ALE hold time (asserted to de-asserted) (DMA Burst)	Output Delay			15	ns
42	ALE	T_{ALHS}	ALE hold time (asserted to 3-State) (Single DMA cycle)	Output Delay			20	ns
43	$\overline{DAS}$	T_{DASS}	DAS setup time from falling edge of T2 SYSCLK (Bus Master)	Output Delay			25	ns
44	$\overline{DAS}$	T_{DASH}	DAS hold time from rising edge of SYSCLK (Bus Master)	Output Delay	5		15	ns
45	DALI/$\overline{DALO}$ BM)/BM1	T_{BMDE}	Bus Master driver enable (from 3-State to driven) (Bus Master)	Output Delay			25	ns
46	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time (Bus Master read)	Output Delay			15	ns
47	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time (Bus Master read)	Output Delay			25	ns
48	$\overline{DALI}$	T_{BMDD}	Bus Master driver disable (from driven to 3-State) (Bus Master)	Output Delay			20	ns

AC TIMING SPECIFICATIONS (Continued) - MK50H25 -25
T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

					MK50H25 -25			
No	**Signal**	**Symbol**	**Parameter**	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
49	$\overline{\text{DALO}}$	T_{ROS}	$\overline{\text{DALO}}$ setup time (Bus Master read)	Output Delay			30	ns
50	$\overline{\text{DALO}}$	T_{ROH}	$\overline{\text{DALO}}$ hold time (Bus Master read)	Output Delay			30	ns
52	$\overline{\text{CS}}$	T_{CSH}	$\overline{\text{CS}}$ hold time		10			ns
53	$\overline{\text{CS}}$	T_{CSS}	$\overline{\text{CS}}$ setup time		10			ns
54	ADR	T_{SAH}	ADR hold time		10			ns
55	ADR	T_{SAS}	ADR setup time		10			ns
56	$\overline{\text{DAS}}$	T_{SDAS}	$\overline{\text{DAS}}$ input setup time (Bus slave)		10			ns
57	$\overline{\text{DAS}}$	T_{SDSH}	$\overline{\text{DAS}}$ input hold time (Bus slave)		10			ns
58	$\overline{\text{READY}}$	T_{RDYS}	$\overline{\text{READY}}$ setup time (Bus slave)	Output Delay			15	ns
59	$\overline{\text{READY}}$	T_{SRYH}	$\overline{\text{READY}}$ hold time after rising edge of $\overline{\text{DAS}}$ (Bus slave read)				15	ns
60	$\overline{\text{READY}}$	T_{RSH}	$\overline{\text{READY}}$ setup time (Bus Master)		18			ns
61	$\overline{\text{READY}}$	T_{SRS}	$\overline{\text{READY}}$ hold time (Bus Master)		10			ns
62	READ	T_{REDS}	READ setup time (Bus slave)		10			ns
63	READ	T_{REDH}	READ hold time (Bus slave)		10			ns
64	$\overline{\text{HOLD}}$	T_{HLDS}	$\overline{\text{HOLD}}$ setup time (Bus Master)	Output Delay			15	ns
65	$\overline{\text{HOLD}}$	T_{HLDH}	$\overline{\text{HOLD}}$ hold time (Bus Master)	Output Delay			35	ns

AC TIMING SPECIFICATIONS (Continued) - MK50H25 -33
T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

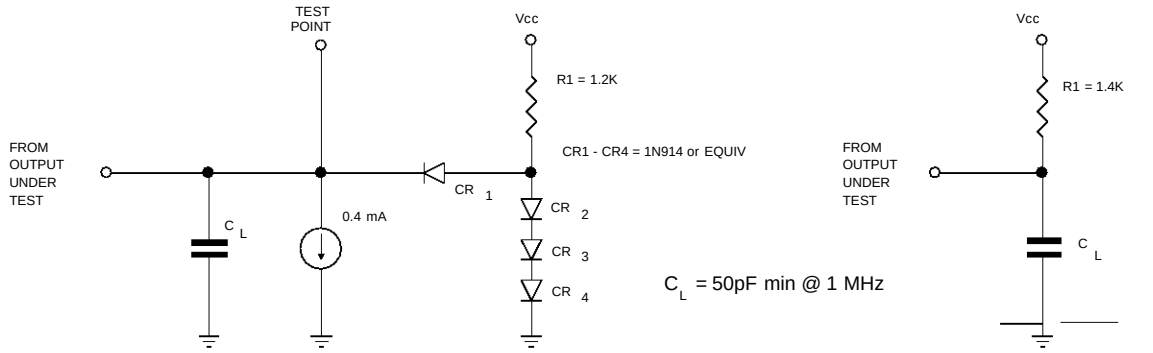
					MK50H25 -33			
No	**Signal**	**Symbol**	**Parameter**	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
13	$\overline{RCLK}$	T_{RCT}	$\overline{RCLK}$ period		20			ns
14	$\overline{RCLK}$	T_{RCH}	$\overline{RCLK}$ high time		8			ns
15	$\overline{RCLK}$	T_{RCL}	$\overline{RCLK}$ low time		8			ns
16	$\overline{RCLK}$	T_{RCR}	Rise time of $\overline{RCLK}$		0		8	ns
17	$\overline{RCLK}$	T_{RCF}	Fall time of $\overline{RCLK}$		0		8	ns
18	RD	T_{RDR}	RD data rise time		0		8	ns
19	RD	T_{RDF}	RD data fall time		0		8	ns
20	RD	T_{RDH}	RD hold time after rising edge of $\overline{RCLK}$		2			ns
21	RD	T_{RDS}	RD setup time prior to rising edge of $\overline{RCLK}$		8			ns
22	ALE/$\overline{DAS}$	T_{DOFF}	Bus Master driver disable	Output Delay	0		20	ns
23	ALE/$\overline{DAS}$	T_{DON}	Bus Master driver enable after rising edge T1 SYSCLK	Output Delay	0		20	ns
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus Master)		0			ns
25	$\overline{HLDA}$	T_{HLAH}	$\overline{HLDA}$ input setup time		10			ns
26	$\overline{HLDA}$	T_{HLAS}	Delay to rising edge HLDA from rising edge $\overline{HOLD}$		10			ns
27	A	T_{XAS}	Address setup time	Output Delay			25	ns
28	A	T_{XAH}	Address hold time	Output Delay			20	ns
29	DAL	T_{AS}	Address setup time	Output Delay			30	ns
30	DAL	T_{AH}	Address hold time	Output Delay	0		20	ns
31	DAL	T_{RDAS}	Data setup time (Bus Master read)		13			ns
32	DAL	T_{RDAH}	Data hold time (Bus Master read)		8			ns
33	DAL	T_{WAH}	Address hold time (Bus Master write)	Output Delay			15	ns
34	DAL	T_{WDS}	Data setup time (Bus Master write)	Output Delay			25	ns
35	DAL	T_{WDH}	Data hold time (Bus Master write)	Output Delay			25	ns
36	DAL	T_{SRDS}	Data setup time (Bus Slave read)				25	ns
37	DAL	T_{SRDH}	Data hold time (Bus slave read)				25	ns
38	DAL	T_{SWDH}	Data hold time (Bus slave write)		10			ns
39	DAL	T_{SWDS}	Data setup time (Bus slave write)		10			ns
40	ALE	T_{ALES}	ALE setup time	Output Delay			25	ns
41	ALE	T_{ALHB}	ALE hold time (asserted to de-asserted) (DMA Burst)	Output Delay			15	ns
42	ALE	T_{ALHS}	ALE hold time (asserted to 3-State) (Single DMA cycle)	Output Delay			20	ns
43	$\overline{DAS}$	T_{DASS}	DAS setup time from falling edge of T2 SYSCLK (Bus Master)	Output Delay			20	ns
44	$\overline{DAS}$	T_{DASH}	DAS hold time from rising edge of SYSCLK (Bus Master)	Output Delay	5		15	ns
45	DALI/$\overline{DALO}$ BM)/BM1	T_{BMDE}	Bus Master driver enable (from 3-State to driven) (Bus Master)	Output Delay			20	ns
46	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time (Bus Master read)	Output Delay			15	ns
47	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time (Bus Master read)	Output Delay			20	ns
48	$\overline{DALI}$	T_{BMDD}	Bus Master driver disable (from driven to 3-State) (Bus Master)	Output Delay			20	ns

AC TIMING SPECIFICATIONS (Continued) - MK50H25 -33
T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

					MK50H25 -33			
No	**Signal**	**Symbol**	**Parameter**	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
49	$\overline{\text{DALO}}$	T_{ROS}	$\overline{\text{DALO}}$ setup time (Bus Master read)	Output Delay			25	ns
50	$\overline{\text{DALO}}$	T_{ROH}	$\overline{\text{DALO}}$ hold time (Bus Master read)	Output Delay			25	ns
52	$\overline{\text{CS}}$	T_{CSH}	$\overline{\text{CS}}$ hold time		10			ns
53	$\overline{\text{CS}}$	T_{CSS}	$\overline{\text{CS}}$ setup time		10			ns
54	ADR	T_{SAH}	ADR hold time		10			ns
55	ADR	T_{SAS}	ADR setup time		10			ns
56	$\overline{\text{DAS}}$	T_{SDAS}	$\overline{\text{DAS}}$ input setup time (Bus slave)		10			ns
57	$\overline{\text{DAS}}$	T_{SDSH}	$\overline{\text{DAS}}$ input hold time (Bus slave)		10			ns
58	$\overline{\text{READY}}$	T_{RDYS}	$\overline{\text{READY}}$ setup time (Bus slave)	Output Delay			15	ns
59	$\overline{\text{READY}}$	T_{SRYH}	$\overline{\text{READY}}$ hold time after rising edge of $\overline{\text{DAS}}$ (Bus slave read)				15	ns
60	$\overline{\text{READY}}$	T_{RSH}	$\overline{\text{READY}}$ setup time (Bus Master)		15			ns
61	$\overline{\text{READY}}$	T_{SRS}	$\overline{\text{READY}}$ hold time (Bus Master)		10			ns
62	READ	T_{REDS}	READ setup time (Bus slave)		10			ns
63	READ	T_{REDH}	READ hold time (Bus slave)		10			ns
64	$\overline{\text{HOLD}}$	T_{HLDS}	$\overline{\text{HOLD}}$ setup time (Bus Master)	Output Delay			15	ns
65	$\overline{\text{HOLD}}$	T_{HLDH}	$\overline{\text{HOLD}}$ hold time (Bus Master)	Output Delay			30	ns

Figure 5a: TTL Output Load Diagram

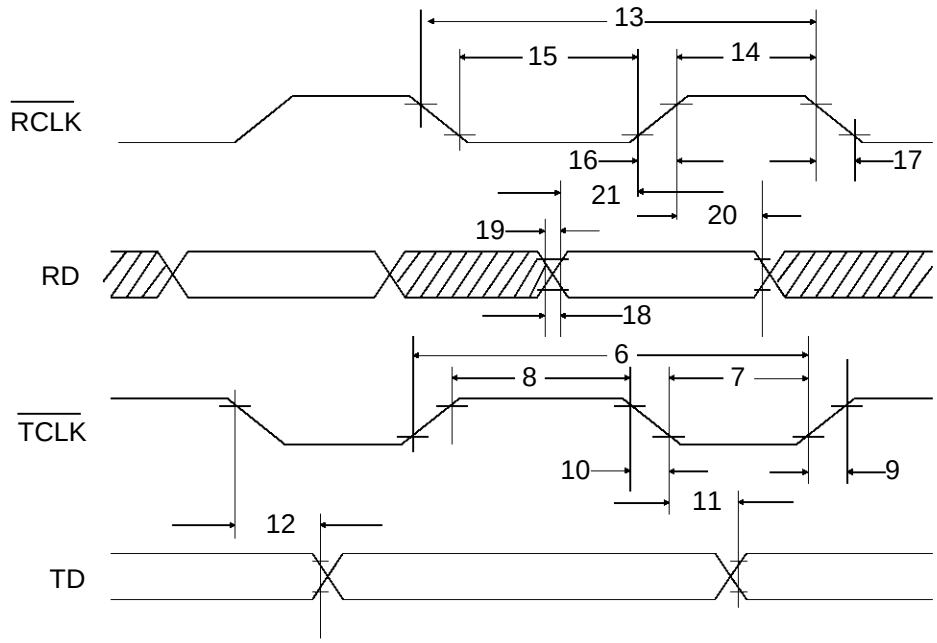
Figure 5b: Open Drain Output Load Diagram



NOTE: This load is used on all outputs except INTR, HOLD, READY.

NOTE: This load is used on open drain outputs INTR, HOLD, READY.

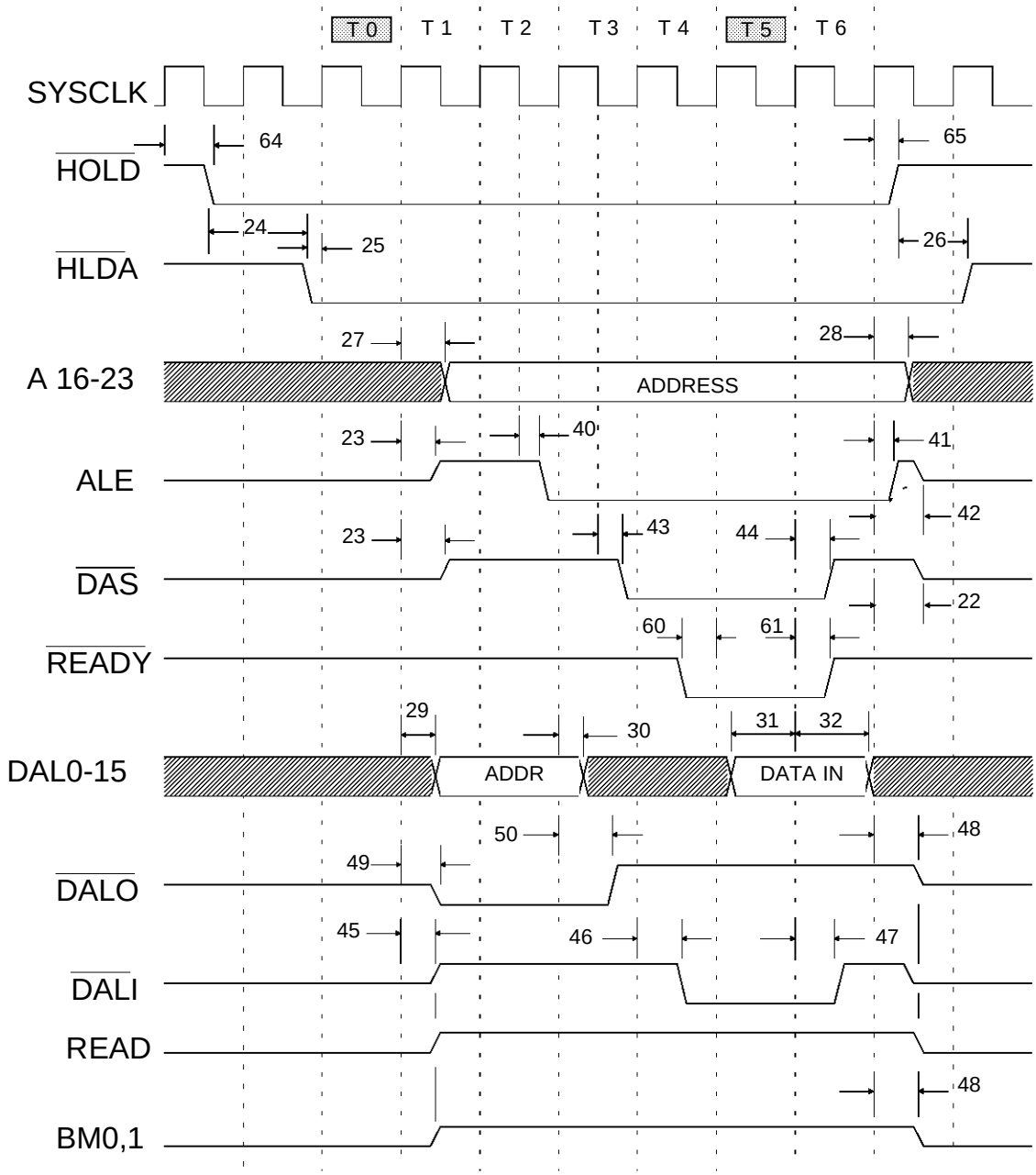
Figure 6: MK50H25 Serial Link Timing Diagram



TIMING MEASUREMENTS ARE MADE AT THE FOLLOWING VOLTAGES, UNLESS OTHERWISE SPECIFIED:

	"1"	"0"
OUTPUT	2.0 V	O.8 V
INPUT	2.0 V	O.8 V
FLOAT	10 %	90 %

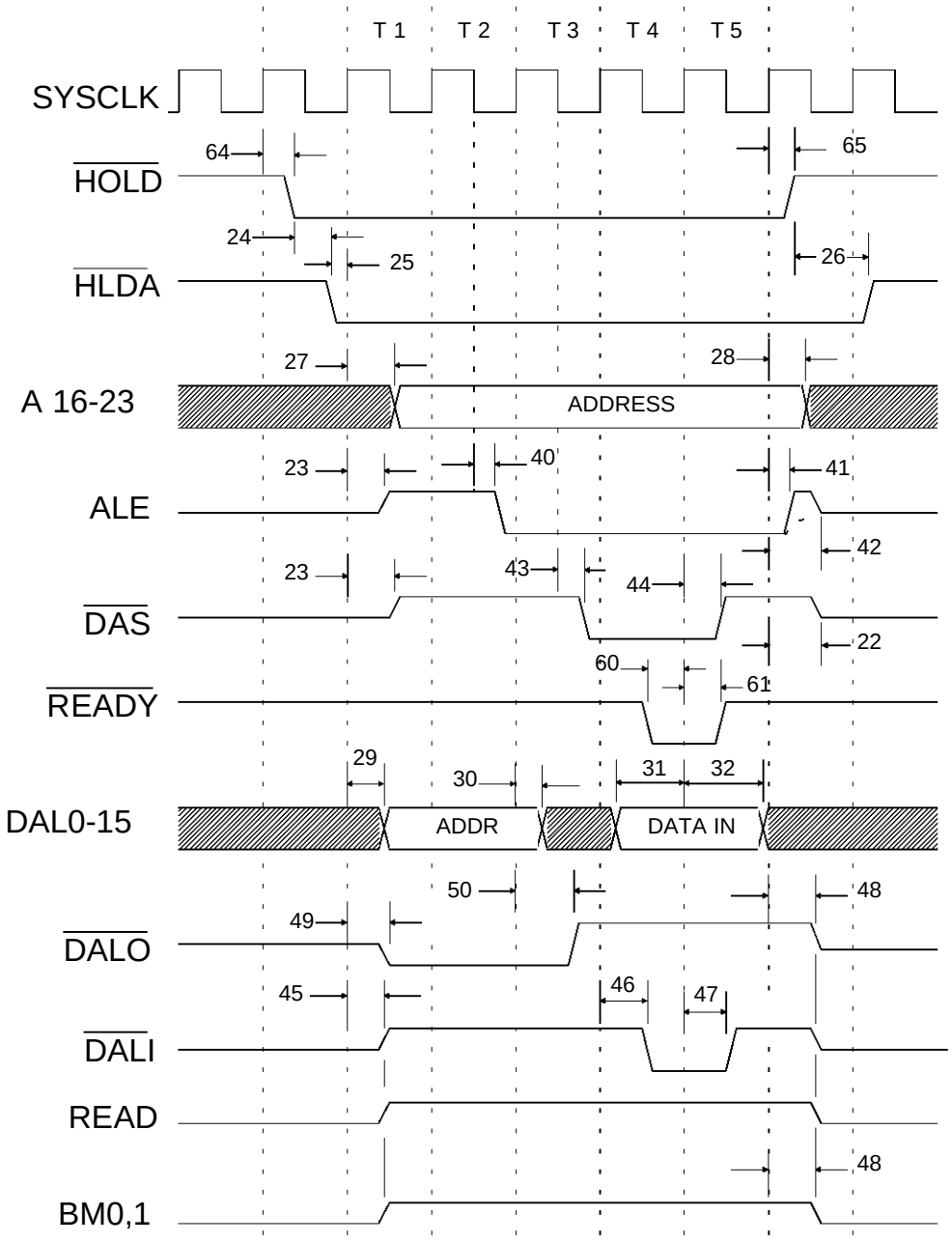
Figure 7: MK50H25 BUS Master Timing (Read) (for CYCLE = 0, CSR2<15>)



NOTES:

1. The shaded SYSCLK periods T0 and T5 will be removed when setting CSR2 bit 15, CYCLE =1 to select the shorter DMA cycle as shown in Figure 7a.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

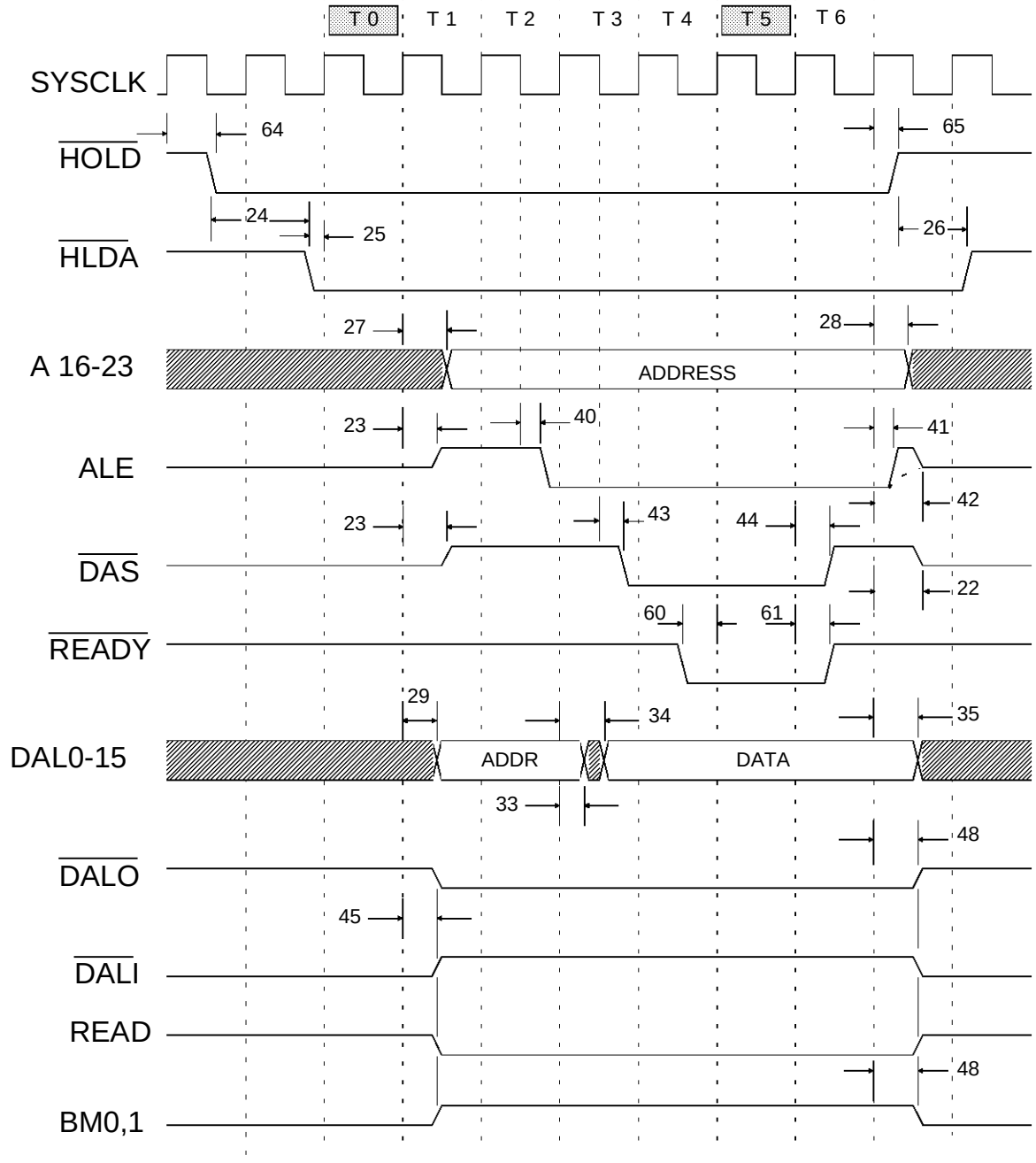
Figure 7a: MK50H25 Reduced Cycle BUS Master Timing (Read) (for CYCLE = 1, CSR2<15>)



NOTES:

1. This reduced DMA Cycle Time is selected by setting CSR2 bit 15, CYCLE =1.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

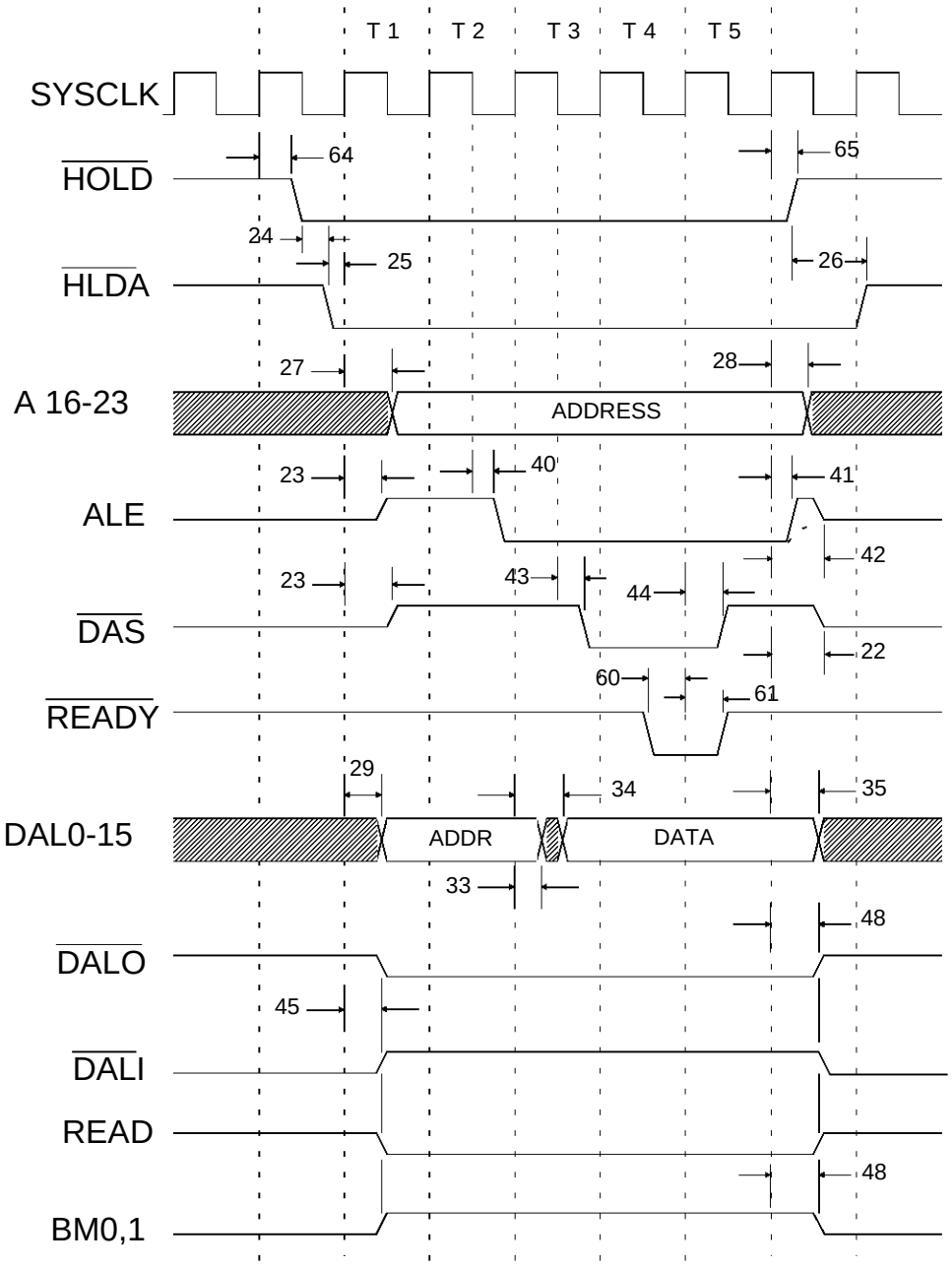
Figure 8: MK50H25 BUS Master Timing Diagram (Write) (for CYCLE = 0, CSR2<15>)



NOTES:

1. The shaded SYSCLK periods T0 and T5 will be removed when setting CSR2 bit 15, CYCLE =1 to select the shorter DMA cycle as shown in Figure 8a.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

Figure 8a: MK50H25 Reduced Cycle BUS Master Timing (Write) (for CYCLE = 1, CSR2<15>)



NOTES:

1. This Reduced DMA Cycle Time is selected by setting CSR2 bit 15, CYCLE = 1. Times T0 and T5 from the standard DMA Cycle are removed for this reduced timing.
2. Output delay times are the maximum delay from the specifed edge to a valid output.
3. The Bus Master cycle time will increase from a minimum, in 1 SYSCLK increments until the slave device returns READY.

Figure 8b: BUS Master BURST Timing (Reduced Cycle - Write)

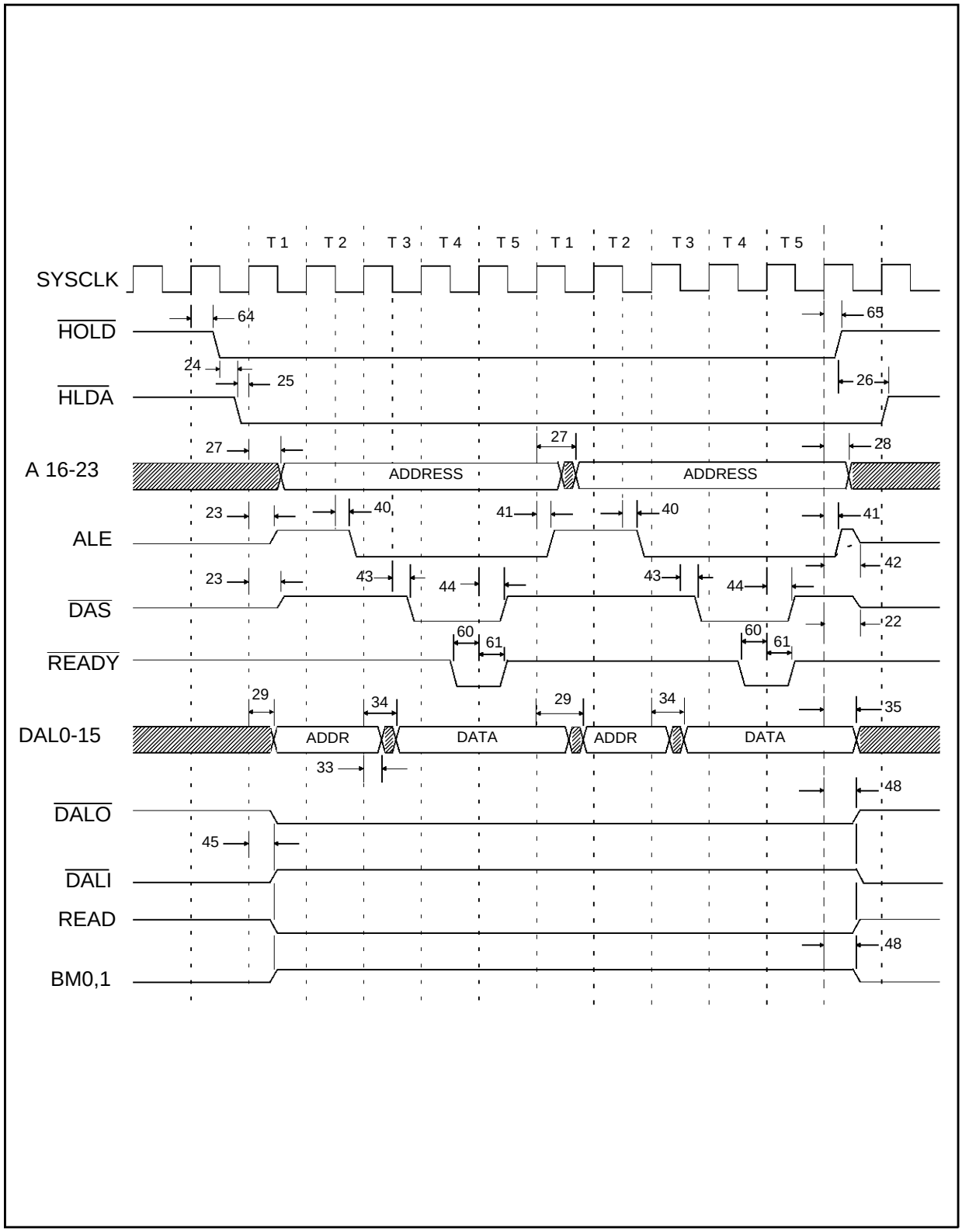
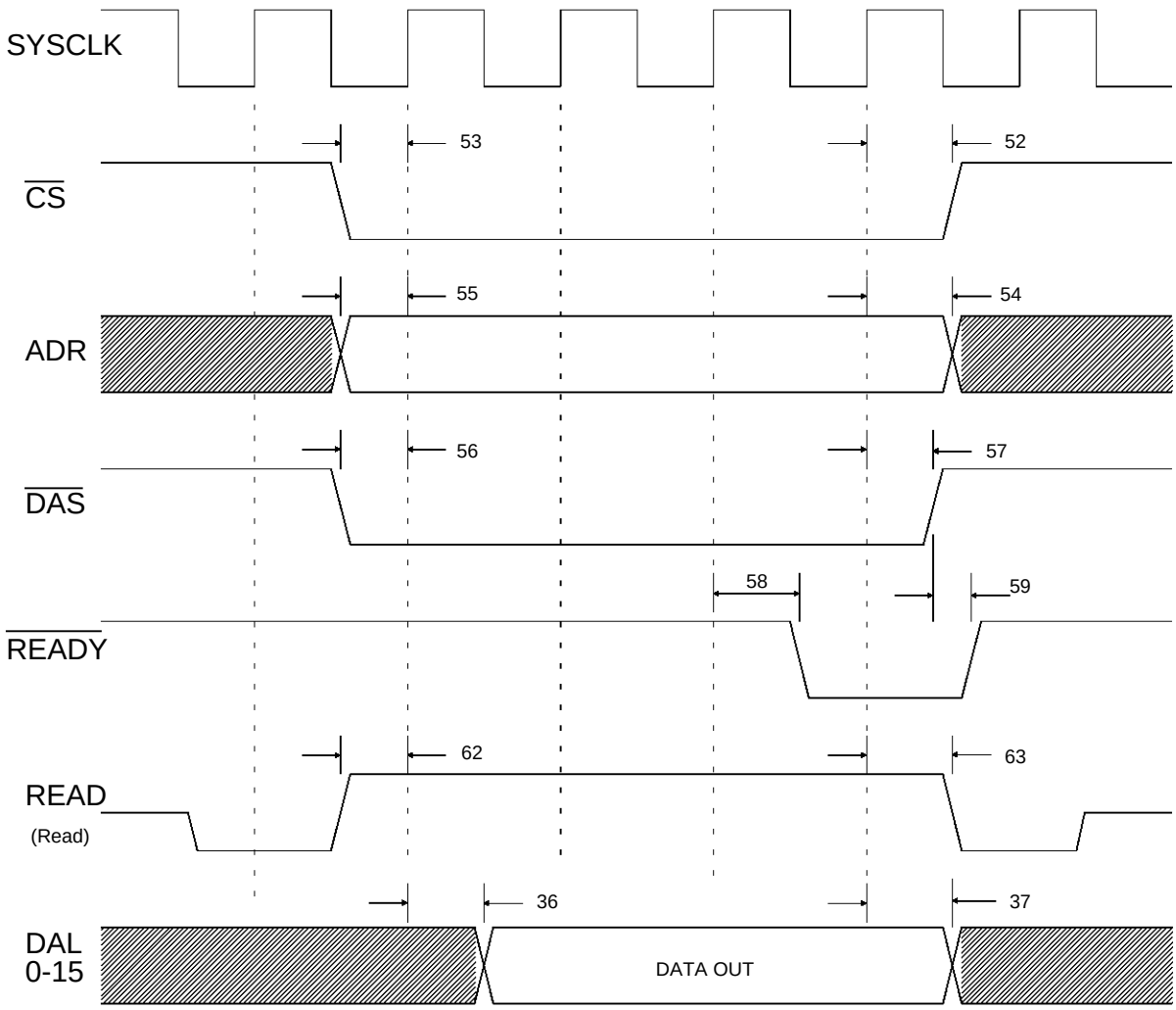
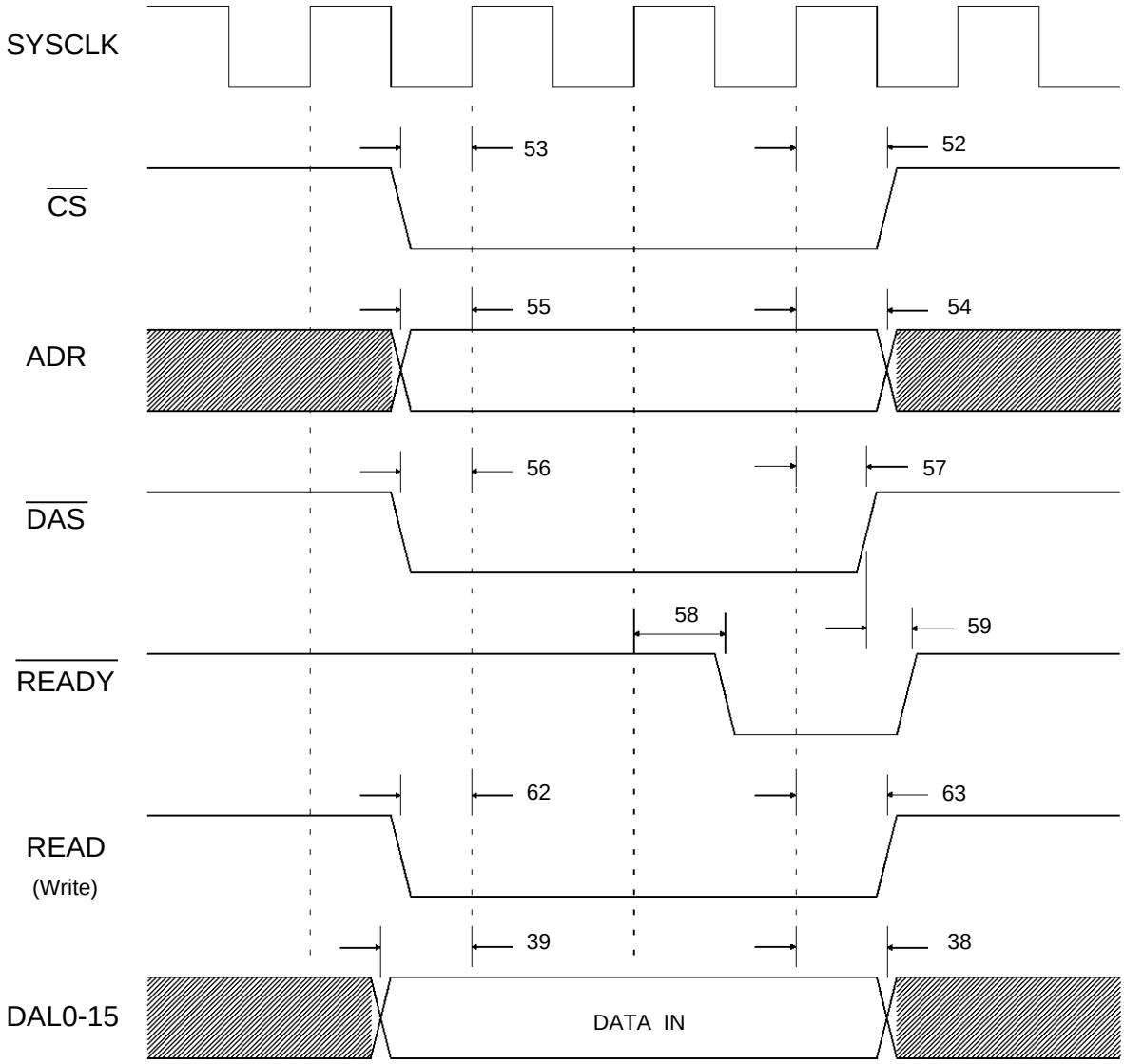


Figure 9: MK50H25 BUS Slave Timing Diagram (Read)



NOTES:
1. Input setup and hold times are in minimum values required to or from the particular edge specified in order to be recognized in that cycle.
2. Output delay times are from the specified edge to a valid output.

Figure 10: MK50H25 BUS Slave Timing Diagram (Write)



NOTES:

1. Input setup and hold times are the minimum values required to or from the particular edge specified in order to be recognized in that cycle.
2. Output delay times are from the specified edge to a valid output.

ORDERING INFORMATION

MK50H25 Q XX

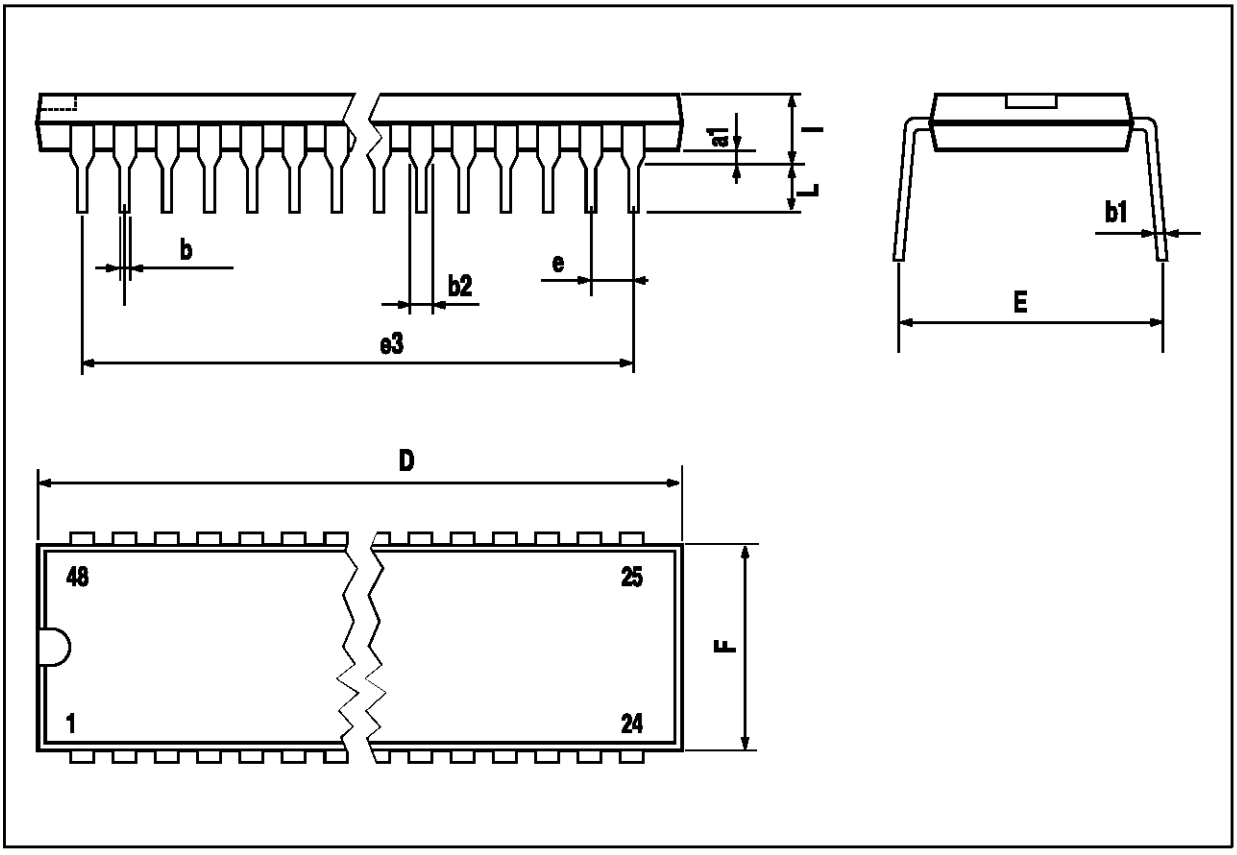
SPEED SORT
16 = 16MHz SYSCLK
25 = 25MHz SYSCLK
33 = 33MHz SYSCLK

PACKAGE
N = Plastic DIP (48 Pins)
Q = Plastic J-Leaded Cip Carrier (52 Pins)
-84Q = 84 PLCC for use with external ROM

PART# PROTOCOL
50H25 = LAPB

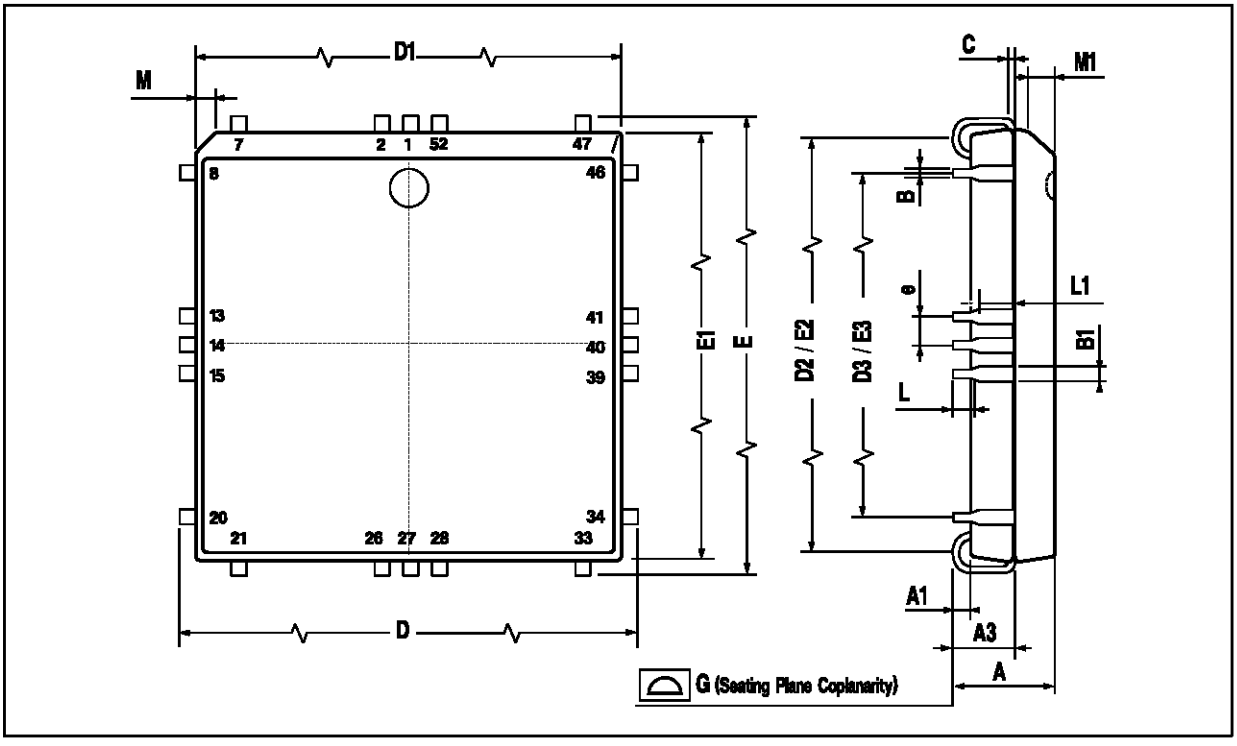
DIP48 PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			62.74			2.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		58.42			2.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	



PLCC52 PACKAGE MECHANICAL DATA

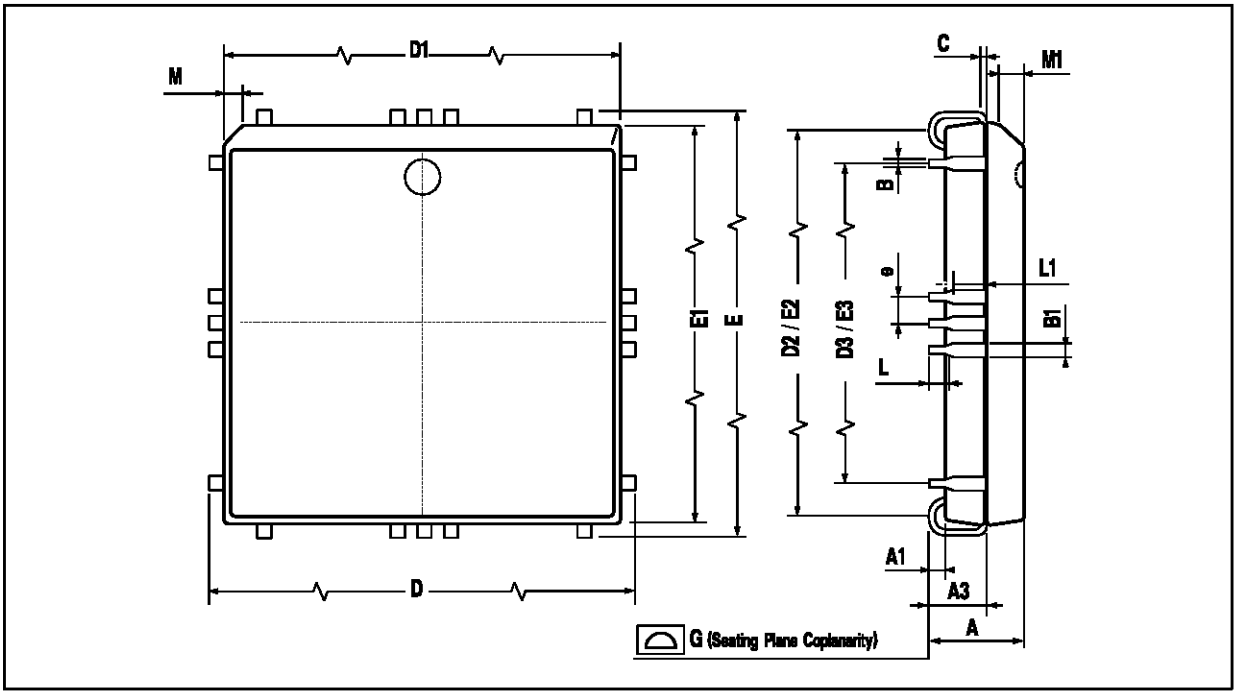
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		4.20	5.08		0.165	0.20
A1		0.51			0.020	
A3		2.29	3.30		0.090	0.13
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
C	0.25			0.01		
D		19.94	20.19		0.785	0.795
D1		19.05	19.20		0.750	0.756
D2		17.53	18.54		0.690	0.730
D3	15.24			0.60		
E		19.94	20.19		0.785	0.795
E1		19.05	19.20		0.750	0.756
E2		17.53	18.54		0.690	0.730
E3	15.24			0.60		
e	1.27			0.05		
L		0.64			0.025	
L1		1.53			0.060	
M		1.07	1.22		0.042	0.048
M1		1.07	1.42		0.042	0.056



PLCC84 PACKAGE MECHANICAL DATA

See following page for PLCC84 pin description

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		4.20	5.08		0.165	0.20
A1		0.51			0.020	
A3		2.29	3.30		0.090	0.13
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
C	0.25			0.01		
D		30.10	30.35		1.185	1.195
D1		29.21	29.41		1.150	1.158
D2		27.69	28.70		1.090	1.130
D3	25.40			1.00		
E		30.10	30.35		1.185	1.195
E1		29.21	29.41		1.150	1.158
E2		27.69	28.70		1.090	1.130
E3	25.40			1.00		
e	1.27			0.05		
L		0.64			0.025	
L1		1.53			0.060	
M		1.07	1.22		0.042	0.048
M1		1.07	1.42		0.042	0.056



MK50H25 PLCC84 Pin Description

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	Vss	43	NC
2	$\overline{\text{EROMEN}}$ - External ROM Enable	44	$\overline{\text{TCLK}}$
3	DAL07	45	DTR
4	NC	46	EROMA0
5	DAL06	47	$\overline{\text{RCLK}}$
6	EROMD11	48	EROMA1
7	DAL05	49	SYSCLK
8	DAL04	50	TD
9	DAL03	51	EROMA2
10	EROMD10	52	DSR/$\overline{\text{CTS}}$
11	DAL02	53	RD
12	DAL01	54	EROMA3
13	DAL00	55	A23
14	EROMD09	56	EROMA4
15	READ	57	A22
16	EROMD08	58	EROMA5
17	$\overline{\text{INTR}}$	59	A21
18	$\overline{\text{DALI}}$	60	NC
19	$\overline{\text{DALO}}$	61	A20
20	NC	62	NC
21	Vss	63	A19
22	NC	64	Vss
23	EROMD07	65	A18
24	$\overline{\text{DAS}}$	66	A17
25	EROMD06	67	EROMA6
26	$\overline{\text{BM0}}$	68	A16
27	EROMD05	69	EROMA7
28	$\overline{\text{BM1}}$	70	DAL15
29	$\overline{\text{HOLD}}$	71	DAL14
30	EROMD04	72	EROMA8
31	ALE	73	DAL13
32	$\overline{\text{HLDA}}$	74	DAL12
33	EROMD03	75	EROMA9
34	$\overline{\text{CS}}$	76	DAL11
35	EROMD02	77	EROMA10
36	ADR	78	DAL10
37	EROMD01	79	EROMA11
38	$\overline{\text{READY}}$	80	DAL09
39	EROMD00	81	EROMA12 (EITest)
40	$\overline{\text{RESET}}$	82	DAL08
41	Vcc	83	$\overline{\text{EROMAEN}}$ - Ext. ROM Address Enable
42	Vss	84	Vcc